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PRINCIPLES OF TOP-DOWN MIXED-SIGNAL DESIGN

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CAD

A. A man who acts with deliberate disregard for another's feelings or rights.

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B. An acronym for Computer-Aided Design.

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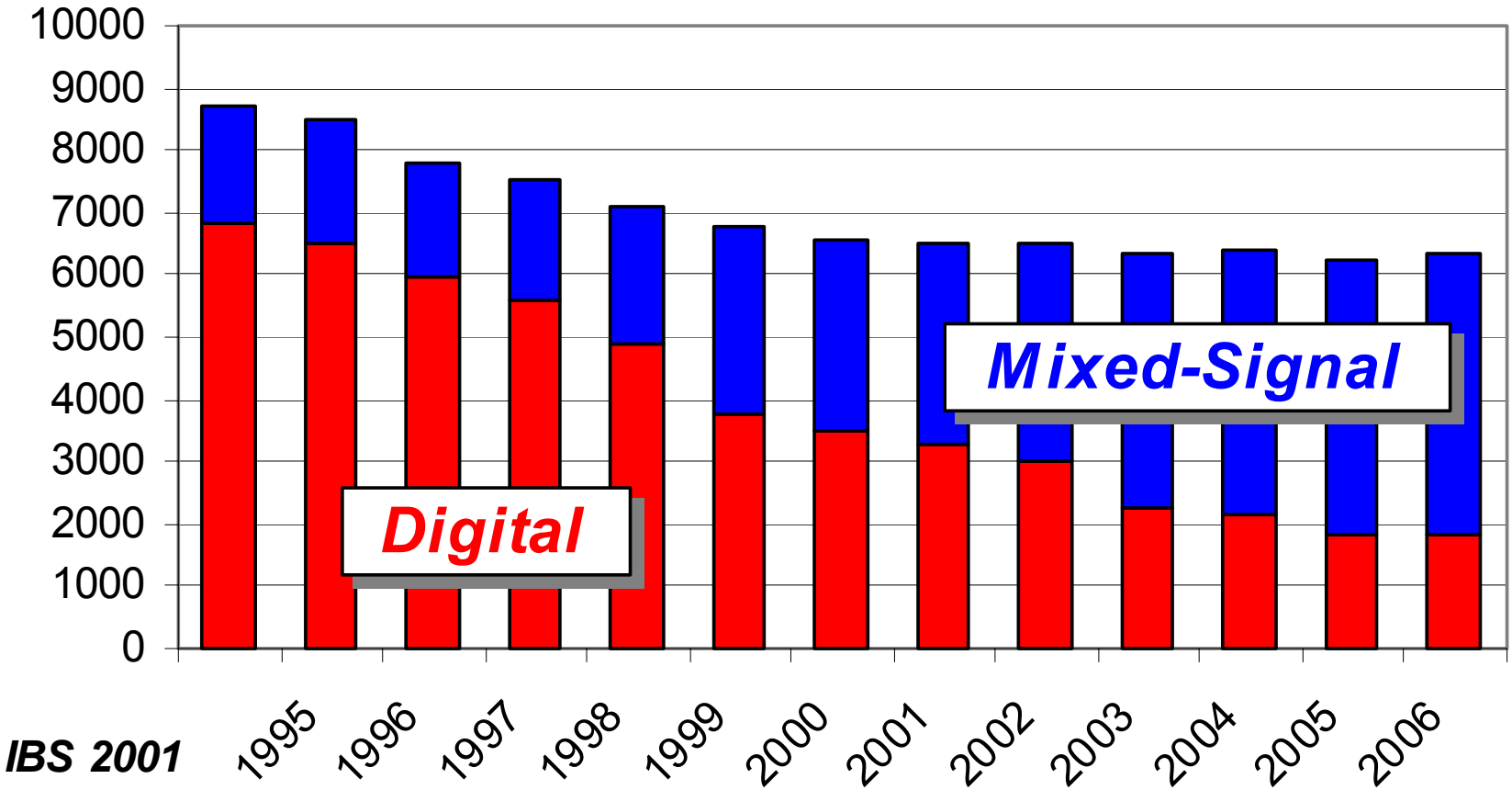
B. Computer-Aided Design.

C. All of the above.

Design Starts



- MS design starts reaches 70% of total by 2006
- MS design starts increasing at 9% CAGR
  - Pure digital falling at 12.5% / year

PERVASIVENESS OF MIXED-SIGNAL DESIGN

- Playing a critical role in every high-value market served by electronics industry
  - Communications: networking and wireless
  - Computing: peripherals, communication in the core
- Traditionally mixed-signal is confined to periphery of systems
  - Used to interface to real world to sense, control, communicate, etc.
  - Amount of periphery is growing
    - Was only periphery of box
    - Increasingly moving to periphery of chip
    - Eventually will move to periphery of block

STATE OF MIXED-SIGNAL DESIGN

- Design methodology characterized by …
  - Heavy dependence on transistor level design
  - Lack of synthesis
  - Need for repeated design and silicon iterations
  - Slow, labor intensive, design cycles
  - *"Analog required 20% of the area, and 80% of the effort and time"*
- Severe time and risk mismatch with digital
  - Acts to discourage integration of analog onto digital chips
  - Makes MS-SOCs both expensive and risky

DIGITAL DESIGN

- Methodology
  - Start with RTL description of finite-state machine
  - Verify with formal verification or logic simulation
  - Synthesize to gate level
  - Lay out
  - Extract, verify and refine
- Result
  - 3 month design cycle typical
  - First time silicon success typical

MIXED-SIGNAL DESIGN

- Methodology
  - System exploration with Matlab, spreadsheets or previous experience
  - Transistor level design of individual blocks
  - Transistor level verification with SPICE
  - Lay out
  - Extraction and final verification with SPICE
- Result
  - 18 month design cycle typical
  - 2-4 respins needed typically

ISSUES WITH MIXED-SIGNAL DESIGN

- Huge schedule and risk mismatch between analog and digital
  - Difficult to justify combining them
  - Problematic if they must be combined
- High risk makes planning difficult
  - When will product be available? When will designers be available?
- Long design cycles imply long time-to-market
  - Cannot quickly react to changes in markets
- Expensive to develop products
- Design talent scarcity exacerbated by low productivity of design process

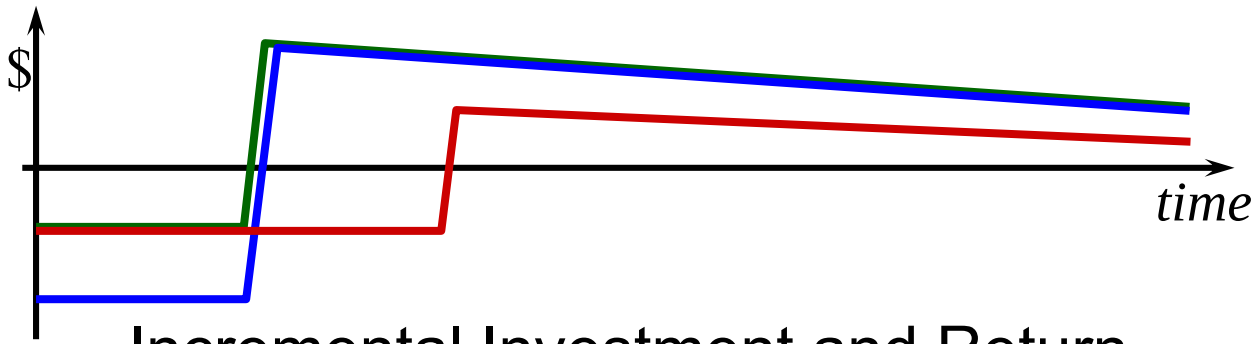
MIXED-SIGNAL DESIGN DRIVERS

- Time to market
- Complexity
- Avoidance of risk
- Reuse
- Increasing fluid design and process requirements
- Gigabit I/O

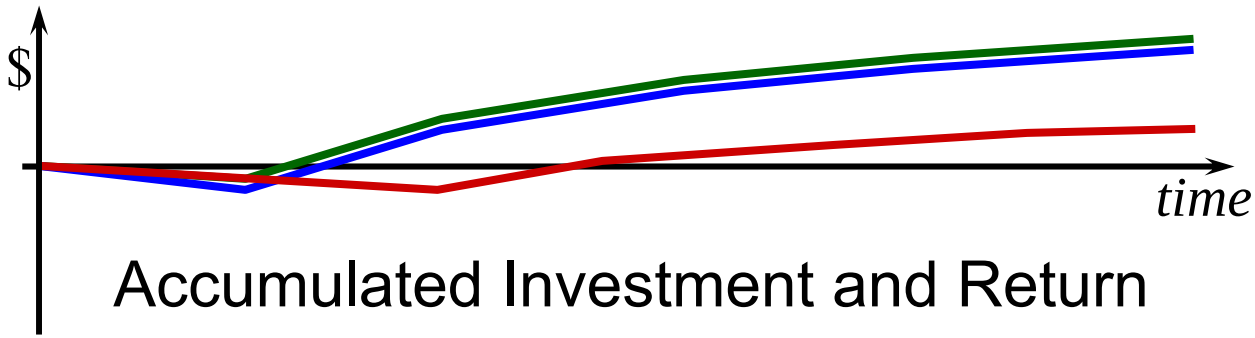
TIME TO MARKET

- Reduced time-to-market required by …
  - Stiff competition
  - Shrinking product lifetimes
- First to market generally captures the lion's share of market
  - Assuming an innovative and well-designed product
- Timely follow-ons keep competitors at bay
  - New features
  - Reduced prices

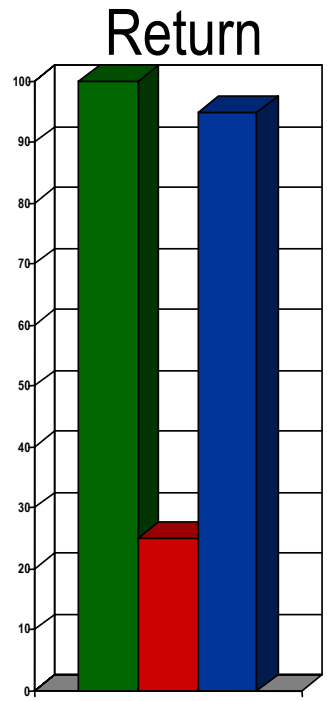
EFFECT ON RETURN OF BEING LATE TO MARKET



Incremental Investment and Return



Accumulated Investment and Return



Efficient and Timely

Inefficient and Untimely

Inefficient but Timely

Timely delivery results in much higher return
It is better to invest heavily rather than risk being late

REDUCING TIME TO MARKET

- Design methodology must
  - Minimize design and silicon iterations
  - Maximize efficiency of each designer
  - Make it possible to efficiently use more designers
    - Reorganize tasks to make them more parallel
    - Eliminate serial dependencies

COMPLEXITY

- Increasing complexity as circuits become larger
  - Increasing integration
    - To reduce cost, size, weight, and power dissipation
- Increasing complexity of signal processing
  - Implementation of algorithms in silicon
    - Adaptive circuits, error correction, PLL's, etc.
- Two forms of complexity combine to overwhelm designers

COMPLEXITY:
IMPROVING CAD IS NOT ENOUGH

"Fundamental improvements in design methodology and CAD tools will be required to manage the overwhelming design and verification complexity"

Dr. H. Samueli, co-chairman and CTO, Broadcom Corp. Invited Keynote Address, "Broadband communication ICs: enabling high-bandwidth connectivity in the home and office", *Slide supplement 1999 to the Digest of Technical Papers*, pp. 29-35, International Solid State Circuits Conference, Feb 15-17, 1999, San Francisco, CA

AVOIDANCE OF RISK

- Recent downturn in economy has exacerbated a fear of risk
  - Respins can overrun development budget
    - Especially with the high-cost of CMOS fabrication
  - Respins can delay revenue, make a product irrelevant
- Result is a fear of mixed-signal design
  - Mixed-signal design is much riskier than digital design

REUSE

- IP reuse — Reuse of individual blocks
  - Process evolution and difficulty of migration limits lifetime of IP
  - This limits additional investment expended to support reuse
  - Which in turn, limits IP reuse
- Derivatives — Reuse of entire systems
  - Current design process creates designs that are difficult to inherit
  - Result is an unpleasant choice
    - Keep team on design to speed derivatives (consumes top team)
    - Assign less talented team on derivatives (chance they could flounder)

INCREASING FLUID DESIGN AND PROCESS REQUIREMENTS

- Time-to-market pressures forcing design process to begin before requirements are set
  - Example: communication standards
- Reuse requires that design be tolerant of changes in process, application
- Design methodology should be adept at handling change
  - Allows changes to be quickly proposed, evaluated, communicated
  - Assures design is thoroughly verified after change occurs

GIGABIT I/O

- High-speed serial I/O is increasingly important in high-performance digital systems
- Cannot be placed on separate chip
- Cannot significantly slow release of SOCs
- This is where immovable object (existing analog design process) meets irresistible force (time-to-market needs of high-value SOCs)
  - Will require a dramatic improvement of analog design process

TRADITIONAL DESIGN METHODOLOGY: BOTTOM-UP DESIGN

- Design starts by partitioning design specifications
  - Perhaps with help of spread sheets or Matlab simulations
- Individual blocks are designed at transistor level
  - Each block is verified as a stand-alone unit against specifications
- Blocks are combined and system is verified at transistor level

BOTTOM-UP DESIGN ISSUES

- For complex designs, greatest impact on performance is usually found at architectural level
  - System-level exploration deemphasized in most bottom-up design
- Once blocks are combined, simulation takes a long time
  - Always limits verification, often results in respins
  - Most errors occur when combining blocks, not adequately verified
- Any errors found when assembling system are expensive to fix
  - Involves redesign of blocks

BOTTOM-UP DESIGN ISSUES (cont)

- Informal, error prone approach to communication employed
  - Any failure in communication likely results in respins
    - Need close contact and intensive communication between designers
  - Limits the number of engineers that can be used effectively
  - Limits ability to spread design team over multiple locations
- Many steps in design process are inherently serial
  - Lengthens time to market

MOVING TO TOP-DOWN DESIGN

- In order to address these issues, many design teams are looking to move to a top-down design methodology
- They are adding a more thorough investigation of system architecture to existing design methodology
  - Use Matlab, Simulink, etc. to investigate system-level trades
- This is widely taken to be top-down design
  - However, this methodology is not very different from bottom-up design
  - Does not address most of the issues with bottom-up design
  - More is needed, more can be done

TOP-DOWN DESIGN
WHAT ELSE IS NEEDED

- Improve communications between members of design team
  - Focus on both current and future members of team (reuse)
- Improve verification
  - Find errors that occur during system assembly
  - Find them early so they can be quickly fixed
- Increase parallelism, reduce number of serial tasks
- Improve designer effectiveness and productivity
- Eliminate respins!

IMPROVING TOP-DOWN DESIGN

A well-designed and effective top-down design process will …

- Progress smoothly from system design to layout without discontinuities (abrupt transitions or “one-way valves”)
  - Discontinuities are an important source of errors
- Naturally formalize and improve effectiveness of communication
- Increase quantity and quality of verification
  - Should move it earlier in design process where fixes are cheaper
- Emphasize use of carrots, de-emphasize use of sticks

PRINCIPLES OF TOP-DOWN DESIGN

- A shared design representation
  - Representation is shared between all team members, design phases
- Every change is verified
  - In context of entire, previously verified, system
- Careful verification planning
  - Risks are identified up front, plans are developed to mitigate risks
- Take an initial quick pass through the entire design process
  - Use abstractions and estimates as needed to include impact of physical design early in the design process
- Executable specifications and plans
  - Scripts and models are preferred over documents

A SHARED DESIGN REPRESENTATION

- Today
  - System designers use Matlab, spread sheets
  - Circuit designers use Verilog, VHDL, or SPICE
  - Use paper to communicate important design requirements
  - Disconnects design process, gap causes errors that force respins
- Using a shared design representation based on Verilog/VHDL-AMS
  - System designer passes models to circuit designers
  - Circuit designers verify their blocks in context of entire system
  - Shared design representation improves communications

EVERY CHANGE IS VERIFIED

- Progressing from system to architectural to circuit to layout …
  - Each change should be verified with mixed-level simulation
  - Individually refine blocks to next lower level
  - Verify by co-simulating block as implemented with rest of system represented using high-level behavioral models
  - Generally, only one or two blocks are at transistor or layout levels at any one time
- Each block is verified in the context of the whole system
  - Easy to see effect of block imperfections on system performance
  - Interfaces are repeatedly tested

CAREFUL VERIFICATION PLANNING

- Existing chips are too large and complex to effectively verify using brute-force simulation at transistor level
- Increase effectiveness of verification with thoughtful strategy
  - Anticipate problems
  - Develop efficient strategies for detecting them early
    - Heavily exploit mixed-level simulation
  - Focus on inter-block problems
- Verification plan includes detailed simulation and modeling plans

AN QUICK INITIAL DESIGN

- Estimate impact of early design decisions on later design stages
- Start with estimates, refine as the detail becomes available
  - Top level behavioral
  - Block level behavioral
  - Block size estimates
  - Initial floor plan
  - Initial routings
  - Parasitic extraction
  - Annotate back to top level simulations
- Avoids redesigns by exposing problems early

EXECUTABLE SPECIFICATIONS AND PLANS

- Written specifications and plans are poorly leveraged
  - Time consuming to write
  - Often ambiguous and out-of-date
  - Often go unread
  - Rarely effective at improving communications between designers
  - Viewed as low value by those that both write and read them
- In contrast, models and scripts are highly leveraged
  - Used on a daily basis and consistently maintained
  - Inherently very specific, eliminates ambiguity that leads to respins
  - Viewed as high value

EXECUTABLE SPECIFICATIONS AND PLANS (cont)

- Models and scripts should be maintained with the design data
  - Single copy, shared between all designers
  - Available to support reuse
    - Validated high-level models available at end of design process
    - These models used to evaluate suitability of blocks for IP reuse
    - Models and scripts help new team members become acclimated
      - Particularly important for derivatives

A RIGOROUS TOP-DOWN DESIGN PROCESS

- A rigorous top-down design process includes these components
  - Simulation and modeling plans
  - System-level exploration and verification
  - Mixed-level simulation
  - Bottom-up verification
  - Final verification
  - Test
- Will resolve all of the issues identified with previous design methodologies

SIMULATION AND MODELING PLANS

- Identify particular areas of concern
  - Develop plans for verifying each area of concern
- Plans specify
  - How tests are performed
  - Which blocks are a transistor level
  - What effects should be include in behavioral models, etc.
- Plans assure
  - Nothing is forgotten
  - Verification occurs as early as possible
  - Verification is efficient as possible
  - Blocks are not over-modeled, run efficiently
  - Reliance on transistor-level final verification is minimized

SYSTEM-LEVEL EXPLORATION AND VERIFICATION

- System designers first choose algorithm, then architecture
- Use system simulators to understand and refine algorithm
  - Matlab, Simulink, SPW, etc.
- Then maps algorithm to a particular architecture
  - Accurately reflect way algorithm is partitioned for implementation
  - Interfaces also chosen to avoid coupling that is hard to predict, control, or model
  - MS-HDL (Verilog & VHDL-AMS) preferred during this phase
  - Use “pin-accurate” models of block to enable mixed-level simulation

SYSTEM-LEVEL EXPLORATION AND VERIFICATION (cont)

- Transition between algorithm and architecture design is currently a discontinuity in the design flow
  - Tools used during algorithm design are different from those used during and after architecture design
  - Operate off of different design representations
- MS-HDLs could be used to design algorithm
  - But they are new, and do not yet have sufficient libraries or application support
  - Alternative is to use a combination system & AMS simulator
    - Such as *AMS Designer* from Cadence – it includes SPW

MIXED-LEVEL SIMULATION

- Starts with executable “pin-accurate” block diagram
  - Every block represented with a behavioral model
  - Block interfaces are carefully modeled
    - Right number of pins, correct polarities, levels, impedances, etc.
  - Behavioral models act as executable specifications for blocks
- Selectively move individual blocks to transistor level
  - Simulator must support both behavioral & transistor simulation
    - Verilog-AMS, VHDL-AMS
  - System acts as a test bench for the block
    - Block is verified in the context of the overall system
    - Allows effect of block performance on overall system to be observed

MIXED-LEVEL SIMULATION (cont)

- Needed to assure accurate refinement to implementation
  - Necessitated by lack of synthesis
  - Assures block interfaces conform to agreements
    - Eliminates a major source of errors that cause respins
  - Moves verification up, making it faster and easier to fix errors
    - Allows verification to be parallelized
- Provides natural and effective way of sharing information
  - Especially between system and block designers
- Only viable approach for verifying complex mixed-signal systems
- Depends on careful verification planning

BOTTOM-UP VERIFICATION

- Update behavioral models after implementation
  - Model “as implemented” rather than “as specified” behavior
  - Updating of models is driven by modeling plan
- Update models during mixed-level simulation (don’t wait to end)
  - Update models as information becomes available
    - From initial transistor schematic, from layout
  - More accurate, more thoroughly verified models
  - Makes mixed-level simulation more effective
    - Don’t make models too slow
- Build and verify abstract models of blocks for IP reuse
  - Allows evaluation of IP by external groups while hiding details

FINAL VERIFICATION

- Extensive transistor-level final verification is generally impossible
  - Even with fast, reduced accuracy, transistor-level simulators
  - Need for it is greatly reduced by mixed-level simulation
- Transistor-level simulation used judiciously
  - As dictated by simulation plan
  - Identify and verify areas of special concern
    - Critical paths, start-up behavior
  - Idea is not to eliminate transistor-level verification, but to maximize its effectiveness while minimizing time doing it

TEST DEVELOPMENT

- Develop and test …
  - Tester programs
  - Built-in self test
  - Scan test
- Starts once executable block diagram available
  - Moves up and parallelizes a serial task that occurred late, acted a gate to release
  - Significantly reduces time-to-production
  - Can find untestable chips earlier
  - Can improve tests, increasing yield

TOP-DOWN DESIGN TEAM

- A large top-down team consists of the following roles and responsibilities
  - Team lead
  - Top-level designer
  - System designer
  - Block designers
  - Modeling engineers
  - Test engineers
  - Senior architect
  - Program manager

TEAM LEAD

- Focus on single project
- Manages schedule & resources
- Acts as technical interface to customers
- Develops simulation & modeling plans
- Manages communications between designers
- Interfaces with design methodology group, responsible for PDKs
- Contributes to architecture, partitioning of block specs, test plan
- Ultimately responsible for technical execution of implementation

TOP-LEVEL DESIGNER

- Works on single project at a time
- Specifies how blocks are assembled
- Owns floorplan, inter-block wiring, top-level schematic
- Responsible for top-level verification and mixed-level simulation
  - Assures changes to block interfaces, updated behavioral models, are properly communicated and employed
- Designs supply, bias, and clock distribution networks
- Typically an experienced block designer
  - Also understands physical design and architecture

BEHAVIORAL MODELING

- Responsibility for writing behavioral models varies with
  - Complexity of project
  - Type of block
- Simple blocks typically written by block designers
  - Use to debug test bench
- Complex blocks written by system designer or modeling engineer
  - Models such as PLL or CDR require specialized knowledge & skill
- System or top-level designers usually create system-level test benches

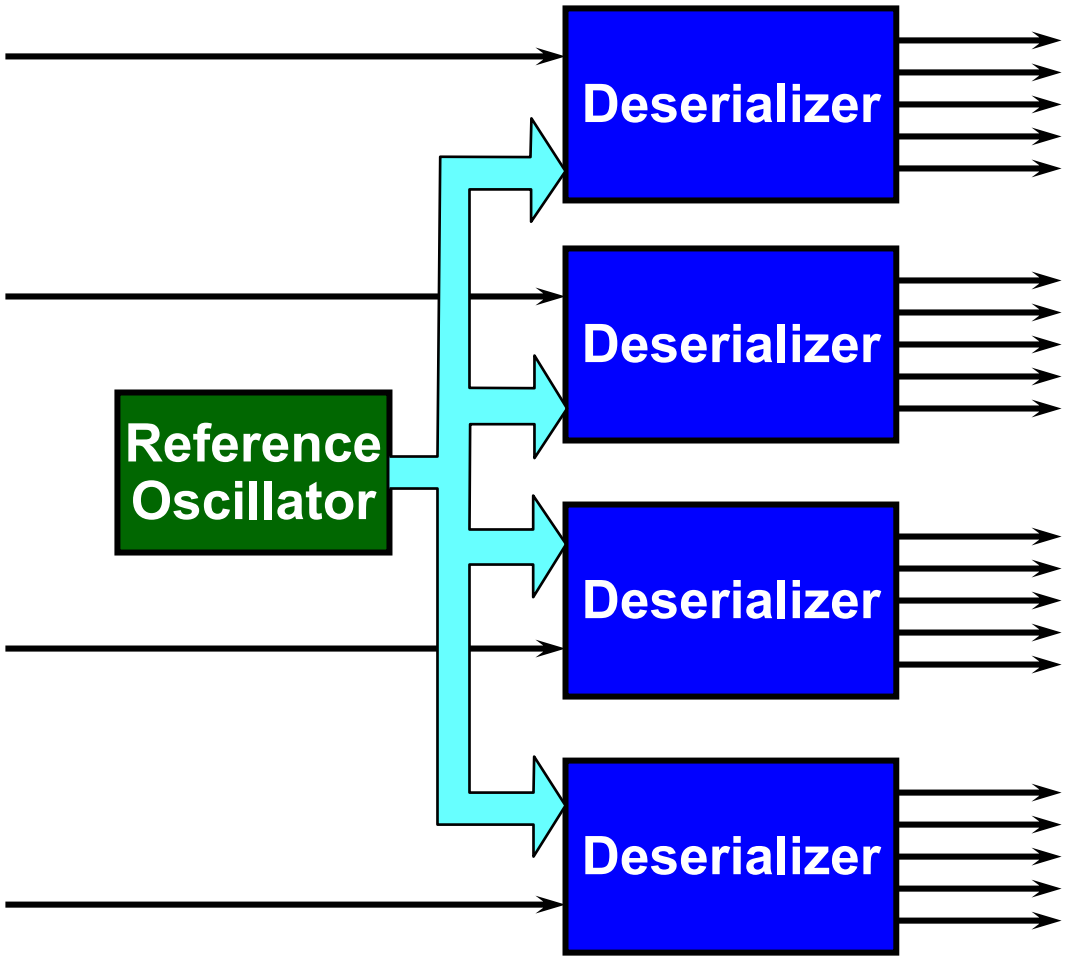
MIXED-SIGNAL HARDWARE DESCRIPTION LANGUAGES

- Verilog-AMS or VHDL-AMS
- Allows co-simulation with behavioral, gate, and transistor levels
- Shared simulator for analog, digital and system designers
- Supports analog event-driven modeling
  - Gives tremendous performance boost to analog behavioral models
  - ADCs, DACs, PLLs, CDRs, modulators, S&H, SC filters, etc.
- Simulators are available
  - Cadence's AMS Designer combines Spectre & NCsim to provide …
    - Verilog-AMS, VHDL, SPICE

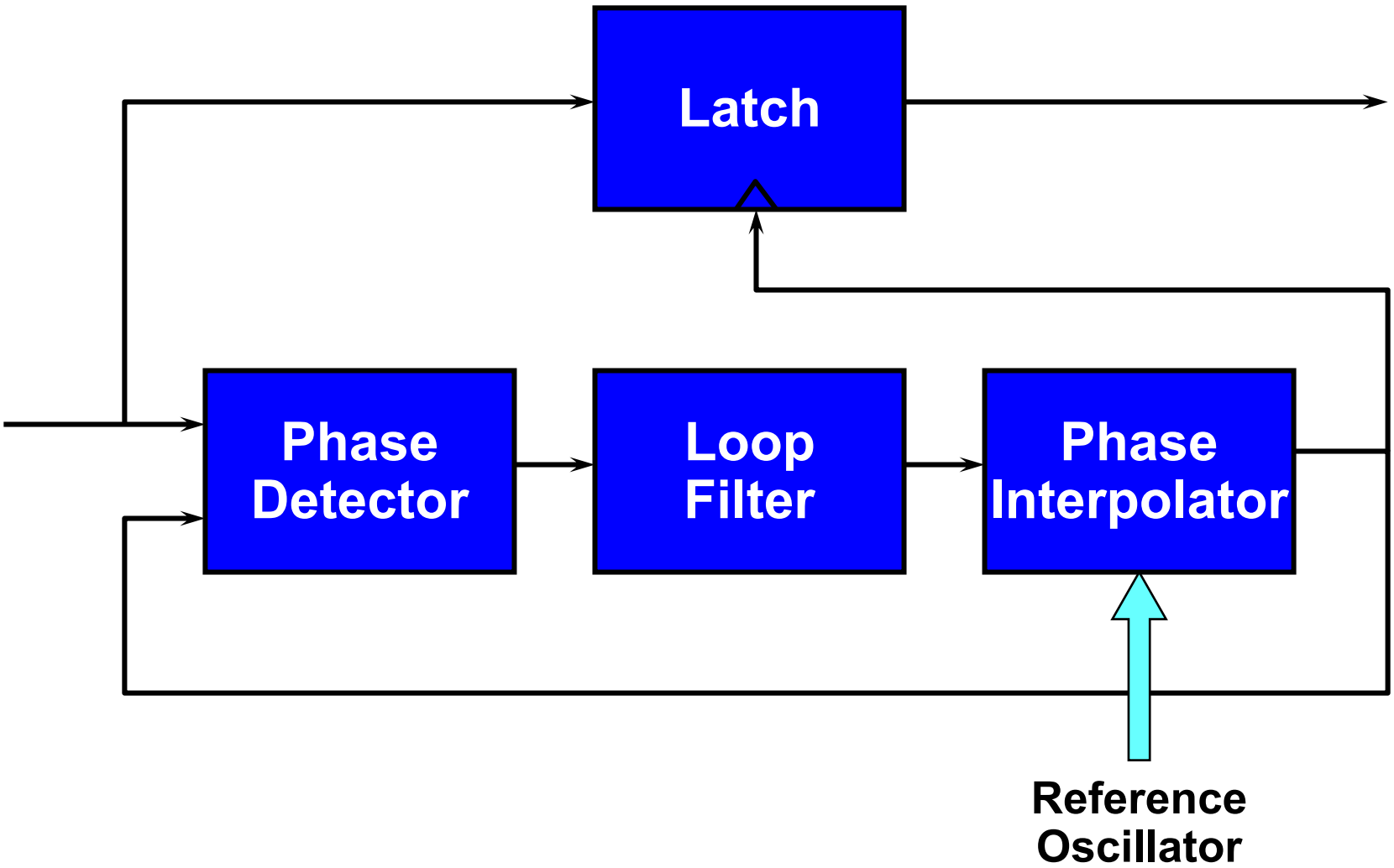
EXAMPLE: SERDES MACRO

- Serdes is a serializer and deserializer combination
- Used for high-speed serial communication
- Serdes Macro is a block that is placed on a chip, generally in a group
- A group of serdes should share a single reference oscillator
  - Natural for serializers, but not for deserializers
  - If each deserializer has its own VCO there is a high likelihood of entrainment (injection locking through coupling)
  - Instead use reference oscillator and phase interpolator
  - Can correct frequency offsets up to ~100 PPM or so

EXAMPLE: DESERIALIZER MACROS



EXAMPLE: CLOCK RECOVERY



EXAMPLE: TDD OF SERDES MACRO
Verification Plan

- Build Verilog model for every cell
  - Assures basic connectivity and functionality
- Use cell characterization for phase detector, divider, serial-to-parallel converter
- Use mixed-level simulation with charge pump & phase interpolator at transistor level
  - Consider jitter in input, data dependent jitter, jitter in reference oscillator, noise in supply and bias lines, killer packets (many bits in a row, all of same value), etc.
- Run simulations for 10-100 corners, choose worst for full transistor level verification
- Run high-level simulation for each of >100 operating modes

EXAMPLE: TDD OF SERDES MACRO (cont)

- Simulation of clock recovery
  - Everything at transistor level: 3-4 days
  - Only phase interpolator at transistor level: 3-6 hours
  - Everything at behavioral level: < 15 minutes
- Share Verilog models with customer
  - Two types: functionality based on Verilog, analog based on SPICE
  - Verilog represents full Serdes, models all kinds of timing effects
    - High level model used verify use of serdes in higher level system
  - Analog only represents amplifier, equalizer
    - Low-level model use when designing boards and packages, design for open eye.

EXAMPLE: TDD OF SERDES MACRO (cont)
Future Improvements

- Move to Verilog-AMS
  - Customer only needs one model
  - Allows more faithful modeling of analog portion of system
    - 200 bias lines
  - Include additional effects
    - Varying input amplitude,
    - Channel model
    - Dispersion
    - AC coupling.
  - Includes effect of programmable gain, programmable equalizer, etc.

TOP-DOWN DESIGN

- More than just adding Matlab simulations to bottom-up process
- Must follow top-down principles to address all issues of BUD
  - Shared design representation
  - Verify every change
  - Plan verification
  - Executable specifications and plans
- Requires substantial investment & commitment from all involved
  - Much easier second time around
  - Provides dramatic returns once mastered

TOP-DOWN DESIGN

- Shorter time to market
  - Fewer design and silicon iterations
  - Allows larger, more dispersed, design teams
  - Reduces serial dependencies, allowing parallel development
- Improves productivity
- Allows more complex designs to be undertaken
- Provides a shorter, more predictable, design process
- Tolerant of late changes to requirements, process
- Encourages and supports reuse

THE DESIGNER'S GUIDE

- A website focused on simulation and modeling for analog, RF, and mixed-signal designers
  - www.designers-guide.com
- Includes articles on analysis, modeling, design, and theory
- Interactive discussion forum where you can ask and answer simulation, modeling, and design related questions
- Contains a special 'by invitation only' paper on top-down design
  - www.designers-guide.com/private/tdd-principles.pdf
  - Please, only for paid attendees of this ISSCC short course

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