VCO Jitter Simulation and Its Comparison With Measurement

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Abstract : We have simulated the phase noise of a voltage controlled oscillator (VCO) using an RF circuit simulator, *SpectreRF*™ [1]. This simulator uses a variation of the periodic noise analysis first proposed by Okumura, et al [2]. It computes the power spectral density of the noise as a function of frequency. By assuming that only white noise sources are present in the oscillator it is possible to derive a simple relationship between the level of the phase noise and the jitter. This excludes flicker noise from consideration, however since flicker noise is a low-frequency phenomenon, excluding it only affects the accuracy of the long-term jitter. We compared the jitter with measurement and found the error to be less than 2 dB. An AHDL model for the VCO that efficiently exhibits jitter in the time domain is included. The model was written in Verilog-A. This model can be used to determine the affect of VCO jitter on a larger system, such as a phase-locked loop (PLL).

1 Introduction

VCOs are circuits that are widely used in phase-locked loops (PLLs), and PLLs are heavily used in communication circuits to implement functions such as clock-recovery circuits and frequency synthesizers. Like all oscillators, the output frequency of a VCO randomly fluctuates as the oscillator responds to noise produced by the electrical devices used to construct the circuit. The output frequency deviation of VCO is usually characterized either as jitter or as phase noise. It has a large influence on the timing accuracy or signal to noise (S/N) ratio of circuits like PLLs. As such, it is crucial to have a method to predict the jitter of a VCO.

There have been several methods proposed for characterizing jitter of oscillators and for predicting the affect of that jitter on the systems that include the oscillator. Demir used such a methodology to predict the affect of oscillator jitter on a PLL frequency synthesizer. He did so by using a transient noise (Tnoise) analysis to predict the noise of each of the blocks that make up the PLL [3]. He then made a few simplifying assumptions that allowed him to convert the noise exhibited by each block to jitter. Finally, he developed behavioral models for each block that efficiently included jitter and simulated the whole system at a high-level using a Monte Carlo analysis. While this is a good approach in concept, Tnoise analysis was never implemented in a commercial simulator and so is not readily available. In addition, as implemented it takes too much simulation time to be practical for realistic circuits. Kundert modified Demir's strategy to make it feasible by replacing Tnoise analysis with Pnoise analysis [4]. Pnoise analysis is implemented in *SpectreRF*™ using fast algorithms [1], making it much more available and practical than Demir's Tnoise analysis.

In this paper, we simulated an existing VCO circuit and compare it with measurement to experimentally verify Kundert's method. We used *SpectreRF*™ Pnoise analysis to compute the phase noise of the VCO. We then convert the frequency-domain phase noise to time-domain jitter. In our comparison to measurement, the error of jitter was less than 2 dB.

Hereafter, we will present a basic theory of phase noise, how to convert phase noise into jitter, and how to write an AHDL model for a VCO that includes jitter. We will also present experimental results to demonstrate the accuracy of the method.

2 Phase Noise

Oscillators exhibit a natural tendency to amplify any noise present near their oscillation frequency. The closer the frequency of the noise is to the oscillation frequency, the greater the amplification. In addition, the nonlinear behavior inherent in any physical oscillator acts to suppress amplitude variations, leaving mainly phase variations. These phase variations are referred to as phase noise. The output of a sinusoidal oscillator can be modeled as

$$v(t) = A\sin(2\pi f_c t + \phi(t)). \quad (1)$$

In this equation, sin() is used as an example and can be replaced by any periodic function. The phase noise is represented by the random process $\phi(t)$, which has

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power spectral density $S_\phi(f_m)$ where f_m is the offset from the carrier frequency. It is difficult to directly measure S_ϕ with a spectrum analyzer, so it is also common to measure oscillator noise in terms of $S_v(f_m)$, the power spectral density of the signal itself rather than the phase of the signal. Generally this is given as $L(f_m)$, the signal noise power in a 1 Hz bandwidth relative to the power in the carrier at the fundamental frequency and has units of dBc/Hz. At frequencies where $S_\phi(f_m)$ is small, it is relatively easy to show that [5]

$$S_\phi(f_m) = 2L(f_m) \tag{2}$$

Suppose noise sources in the oscillator are restricted to being white (i.e., no flicker noise). Then close to the carrier the phase noise is proportional to $1/f_m^2$. If flicker noise sources are present in the circuit, then the low frequency flicker noise is modulated up to the oscillation frequency and amplified, with the result that for small f_m the noise power is proportional to $1/f_m^3$ [6].

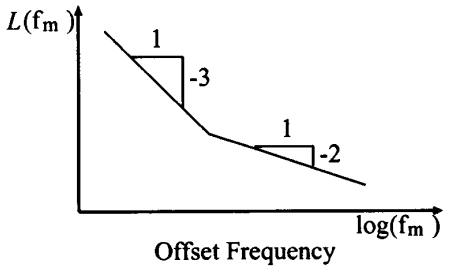

Figure 1: $L(f_m)$vs. offset frequency

We first start from a phase noise simulation. There are several circuit simulators that can be used to analyze noise. The most basic ones are SPICE and its derivatives. Their noise analysis is an application of small signal analysis about a fixed operating point. In a VCO, the operating point is periodic and the noise varies strongly with the operating point, so we need a simulator that can calculate noise about a time-varying operating point. Demir's Tnoise analysis [7] is a conceptually a solution, but as we mentioned before it is not readily available. Harmonic balance simulators [8] are also candidates, but they tend to struggle in terms of both accuracy and convergence because of the strongly nonlinear nature of oscillators.

In this paper, we used *SpectreRF*™for the phase noise calculation. It linearizes the circuit at every time step in a given period and accumulates the contributions from every noise source and over every time point to compute the total noise. It accurately takes into account the effect of the large oscillation signal as it modulates the noise generated by bias dependent noise sources and the characteristics of the nonlinear devices, thereby causing the noise to be mixed about in frequency. It assumes that the noise is small, which is true except at frequencies very close to the oscillation frequency.

3 Converting Phase Noise to Jitter

Phase noise is defined in the frequency domain, while jitter is defined in the time domain. Phase noise and jitter are different ways of characterizing the same underlying phenomenon and, given a simplifying assumption, there is an easy way to convert from one to the other.

As already explained in section 2, if we assume only white noise sources, phase noise $L(f_m)$ is proportional to $1/f_m^2$. Now, define a such that

$$L(f_m) = \frac{a}{2}\frac{(2\pi f_c)^2}{(2\pi f_m)^2} \tag{3}$$

where, f_c is the carrier frequency. Then, a is related to the jitter over a single cycle as follows [3]

$$J = \sqrt{aT} \tag{4}$$

where $J = \sigma(T) = \sqrt{\text{var}(T)}$.

J is computed by performing a Pnoise analysis for the oscillator over a range of frequency. A frequency is chosen where the noise is close to its $1/f_m^2$ asymptote, and the noise power at that frequency is use to compute J using (3) and (4).

For oscillators that are subject to only white noise sources, the variation in the length of one cycle is independent of the variation in the length of a different cycle. As such, the variance of the length of several cycles grows linearly with the number of cycles. Thus,

$$J_i = \sqrt{i}J \quad for \quad i = 0, 1, 2, \cdots \tag{5}$$

where J_i is the standard deviation of the length of i adjacent cycles. If we plot the logarithm of J_i versus the logarithm of i, the slope is 1/2 as shown in Fig. 2.

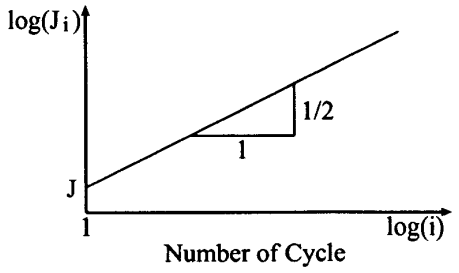

Figure 2: Jitter in the length of i adjacent cycles.

4 VCO AHDL Model With Jitter

Simulating PLLs at the transistor level is very time consuming because they generally take hundreds or thousands of cycles to reach steady-state. However, the situation is much worse when simulating frequency

synthesizers because they often employ frequency dividers with large divide ratios in the feedback path. In this case, one typically needs N times as many cycles to reach steady-state, where N is the divide ratio of the divider. The only practical way of simulating such circuits is using abstract behavioral model.

Here, we give an AHDL model for a VCO that has jitter as an external parameter. This model generates pulses at a rate that is proportional to the input voltage. It models jitter by randomly varying the period of each pulse. This is efficient because it does not create any additional events to simulate, it simple changes the time at which events occur. Thus, models with jitter run as efficiently as those without jitter.

Here, we show a Verilog-A description example for VCO.

```
// Voltage Controlled Oscillator with Jitter

`include "discipline.h"
`include "constants.h"

module vco (out, in);

input in; output out; electrical out, in;

parameter real Vmin=0;
parameter real Vmax=Vmin+1 from (Vmin:inf);
parameter real Fmin=1 from (0:inf);
parameter real Fmax=2*Fmin from (Fmin:inf);
parameter real ratio=1 from [1:inf);
parameter real Vlo=-1, Vhi=1;
parameter real tt=0.01*ratio/Fmax from (0:inf);
parameter real jitter=0 from [0:0.25/Fmax);
parameter real ttol=1e-6/Fmax from (0:1*ratio/Fmax);

real freq, phase, dT;
integer n, seed;

analog begin
  @(initial_step) begin
      seed=-493;
  end

  // compute the freq from the input voltage
  freq = (V(in) - Vmin)*(Fmax - Fmin)
       / (Vmax - Vmin) + Fmin;

  // bound the frequency (this is optional)
  if (freq > Fmax) freq = Fmax;
  if (freq < Fmin) freq = Fmin;

  // add the phase noise
  freq = freq/ratio;
  freq = freq/(1 + dT*freq);

  // phase is the integral of
  // the freq modulo 2 pi
  phase = 2*`M_PI*idtmod(freq, 0.0, 1, -0.5);

  // update jitter twice per period
  @(cross(phase + `M_PI/2, +1, ttol) or
    cross(phase - `M_PI/2, +1, ttol)) begin
    dT = sqrt(2*ratio) * jitter
                       * $dist_normal(seed,0,1);
    n = (phase >= -`M_PI/2) && (phase < `M_PI/2);
  end

  // generate the output
  V(out) <+ transition(n ? Vhi : Vlo, 0, tt);
end
endmodule
```

The oscillation frequency of the VCO is directly dependent on input voltage. The phase of the VCO is computed by integrating the frequency. We are only interested in the phase modulo 2π, and if we used a simple integrator, the phase would tend to infinity, which could cause numerical problems in the simulator. Instead, we use a special function of Verilog-A, `idtmod()`. This function combines an integrator and a modulus operation and is used to efficiently model VCOs without numerical problems. In this example, the output wave is a pulse, but it is possible to use a sinusoid if needed.

Frequency division ratio [ratio] is one of the external parameters for the VCO model. Specifying a value greater than one modifies the output frequency and jitter in the same way that would result if the VCO were followed by a jitter-free frequency divider.

Jitter is defined as the standard deviation of the oscillation period, but in this AHDL implementation, jitter is implemented by dithering the oscillation frequency. The relation between jitter J and oscillation frequency f_i is as the follows.

$$f_i = \frac{1}{T + \Delta T_i} = \frac{f_c}{1 + \Delta T_i f_c} \qquad (6)$$
$$\Delta T_i = J\delta_i$$

where, $f_c = 1/T$ is the oscillation frequency and δ_i is a white Gaussian random process. The multiplier of $\sqrt{2}$ in AHDL description is present because each period is divided into two subperiods, the length of each is independently randomly varied.

We used this AHDL model for the VCO jitter simulation.

5 Experimental Results

In order to check the validity of our method, we applied it to a $0.35\mu m$ CMOS 15-stage voltage controlled ring oscillator. The measured phase noise ($L(f_m)$) is shown in Fig. 3, here we used a spectral analyzer to measure a VCO oscillating at 70 MHz.

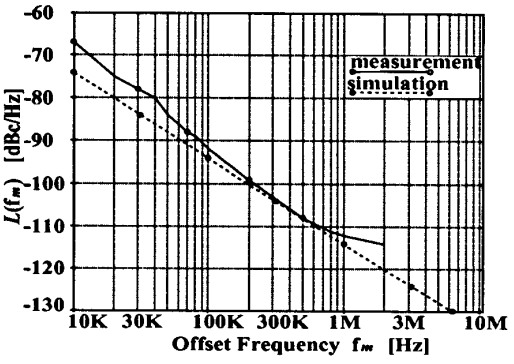

Figure 3: Phase noise vs. offset frequency.

As we explained in sec. 3, we have not yet included flicker noise in (4), the equation that converts phase noise amplitude to jitter. So, we also did not use flicker noise parameters in the MOS model. Thus, we can see some uplift around the oscillation frequency for the measured curve due to flicker noise, but for the simulation curve we see just the slope of 2 due to white

noise only. For a frequency region from 100 KHz to 1 MHz, there should be a very limited influence of flicker noise, so the measurement and the simulation match well. We also show the same comparison of $L(f_m)$ for the two different oscillation frequencies in Tab.1. This shows that the method gives good results

Carrier Frequency[Hz]	Measurement [dBc/Hz]	Simulation [dBc/Hz]
10M	-108	-111.3
70M	-108	-107.8
100M	-108	-108.2

Table 1: Comparison of $L(f_m)$

at any oscillation frequency.

Next, we measured the VCO jitter directly on a digital oscilloscope. The jitter in the length of N adjacent cycles at 70 MHz is plotted on Fig. 4.

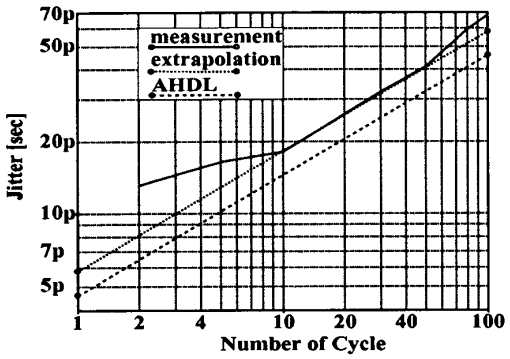

Figure 4: Jitter at $N'th$ cycle

The 3 curves in Fig.4 show the measured and simulated jitter (AHDL-level simulation) in the length of N cycles and the line from the measured jitter extrapolated from the region where the flicker noise is considered small. We can calculate the jitter for one cycle from the extrapolated line in Fig.4 and compare it with the simulated jitter in the Tab.2. The result

Carrier Frequency[Hz]	Measurement [psec]	Simulation [psec]	Error [dB]
10M	72	60.9	1.45
70M	5.8	4.6	2.01
100M	3.2	2.65	1.63

Table 2: Jitter comparison for the first cycle

indicates that the error of simulated jitter is less than or equal to 2 dB which is satisfactory for practical use. As for the AHDL jitter modeling, we confirmed that the jitter in the length of N cycles does indeed vary with $\sqrt{N}$, as expected.

6 Conclusion

We have simulated a VCO jitter. The error from a real measurement was less than 2 dB. And in the VCO simulation at AHDL level including a behavior level jitter model, we checked that the jitter in the length of N cycles is $\sqrt{N}$ times larger the jitter of just one cycle.

This result strongly encourages us to do PLL jitter simulation. But, we need to develop a jitter model that handles flicker noise in the next step toward a complete PLL jitter simulation.

7 Acknowledgments

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