A Design System for RFIC: Challenges and Solutions

Paolo Miliozzi, Ken Kundert †,
Koen Lampaert, Pete Good and Mojy Chian
Conexant Systems, Inc., Newport Beach, CA
† Cadence Design Systems, San Jose, CA

Abstract

The past few years have witnessed an explosion of interest in radio frequency integrated circuits (RFIC's). The expansion of the market for wireless communication devices has given a tremendous push to the development of a new generation of RFIC products, where more and more functions are integrated on the same chip. In this fast-growing environment where time-to-market constraints force tight schedules, having a good design methodology, innovative CAD tools and a well-integrated design system are key factors to success.

In this paper, we describe a Design System developed to provide the designer with everything necessary to accurately predict the behavior of RFIC devices, including layout and package parasitic effects. We show the importance that a well-defined and integrated system has on the final goal of obtaining a manufacturable design that meets specifications at minimum cost and in the minimum time. A close link between schematic, models and layout is of paramount importance to ensure the accuracy needed for RF design. We give an overview of the advanced methods and tools currently available for simulation and noise analysis of RF devices. Finally, we show a couple of design examples that have obtained first-silicon success.

1 Introduction

In recent years, RF design has undergone a paradigm shift as more and more RF functions have been integrated on a single chip and the number of discrete components has decreased. Traditional discrete designs are quickly reaching the physical limits of size, parasitics, and electrical performance. Moreover, while in the past the wireless market was dominated by the relatively slow-growing military and cable television industries, its new consumer nature forces designers to seek more integrated solutions as opposed to the bulky, expensive, and power-hungry ones previously developed.

Being able to place many RF and IF subsystems on the same die promises dramatically smaller size, greater manufacturability, higher performance, and lower power consumption. This trend is more evident in the low-power segment of the wireless communications market, which includes handsets for cordless and cellular phones, pagers, and the more recent BlueTooth standard (See paper in this issue), where more compact solutions are needed to accommodate the ever-growing demand for lighter and cheaper products. Even though RF designs contain fewer devices compared to digital chips, they are inherently more challenging as very little automation is available for the design process. Moreover,

RF devices are typically pushed to their performance limits, thus all the non-linearities and second order effects need to be taken into account.

Consider, as an example, the Super-Hetherodyne transceiver depicted in Figure 1. This transceiver is the combination of several integrated circuits built using different techonologies: bipolar, *GaAs* and ceramic SAW filters are used for the RF section, bipolar for the IF section and CMOS for base-band. This design partitioning is now starting to change thanks to technology advances that make it possible to extend the range of usability of the less expensive CMOS technology. A good overview of the technology choices for RFIC can be found in [1].

Historically, IC and RF designers have used different design methodologies, tools and practices. Traditional analog designers have enjoyed an integrated front-to-back IC design system. On the other hand, RF designers, with a discrete design background, have used board-level CAD design tools. With IC applications approaching several GHz, and the appeal of monolithic design because of the growing device speed, silicon is bridging the gap between traditional low-frequency analog design and discrete RF design, bringing the 2 worlds to converge in order to provide a better and cheaper solution for consumers.

Many of the limitations of IC processes are well known. These involve the inability to economically integrate high value capacitors and resistors, relatively poor (typically $> 10\%$) absolute error tolerances of component parameters, and limited choice of device types. In addition to these limitations, the RFIC designer must also be concerned with parasitics associated with the substrate, the general lack of high quality passive components, and package parasitics.

Moreover, tight schedules imposed by severe time-to-market constraints, make prototyping impossible and urge designers to seek validation of their design from accurate and extensive simulation.

In order to overcome all these problems, RF designers must rely on a Design System that allows them to accurately predict the behavior of their devices under their normal working conditions.

The paper is structured as follows: Section 2 gives an overview of the parts that compose a Design System for RF and focuses on the importance that effective synchronization and coordination between different contributors has for the success of a design. In Section 3 the issues involved in device modeling for RF are described. An in-depth overview of the various simulation methods currently available (e.g. spice, shooting-methods and harmonic balance), is given in Section 4. Section 4 also addresses the subject of noise analysis. This is an area where CAD tools can play a major role helping designers reduce their margins and obtain better performance with lower power consumption.

In Section 5, techniques to automate the layout generation of devices are described. Also, a methodology is presented to retarget a design (template) from one set of specs to another and from one technology to another. In Section 6 the importance of keeping a very tight link between what is simulated and what is laid out so that pre- and post-layout simulations track each other is underlined.

Finally, in Section 7 we show a couple of RFIC designs that have gone through the design cycle and obtained first-pass silicon success as a result of accurate process characterization, noise prediction, device & package models, and appropriate simulation engines in this Design System.

2 Design System

A Design System provides the designer with a comprehensive set of tools, libraries and methodologies that cover an entire design flow. Moreover it is a framework within which process developers, device modeling people, IC designers, package developers and layout designers can exchange information and interact with one another for the common goal of minimizing both the power consumption and time-to-market of every design.

We can divide a Design System in the following main components:

- Design Environment;
- Design Kits;
- Design Methodology associated with a Tool Flow;

Synchronization, testing and release mechanisms are very important aspects of a DESIGN SYSTEM and its components.

A wide portfolio of communication systems has very different technology requirements. To implement the transceiver shown in Figure 1 many different technologies are needed. Hence, many processes need to be managed which may be at different stages of their development. Some of them may be very mature and require very little or no modifications. When working on applications that require a cutting-edge process, the process development and design are done concurrently. This has the advantage that complex test circuits can be available at early stages of the process development, providing feedback for the fine tuning of process parameters. In these cases, since the process is not yet stable, many changes may take place during the design. These changes need to be passed on to designers in a timely manner while keeping the design system consistent. In order for this type of concurrent engineering to be succesful, it is very important to have synchronization mechanisms in place between contributors. This is one of the main factors behind the success or the failure of a design.

Most of the time, a complex design is not carried out by a single design team, but rather by many design teams working in different geographical locations and even different time zones. In these cases the importance of having a common DESIGN SYSTEM is clear. Since the data structure is the same everywhere, synchronization among all sites can be easily accomplished by broadcasting nightly the changes that have occurred.

2.1 Design Environment

Defining a common design environment is necessary to allow seamless interaction between users and tools and between one tool and another. This has the added advantage that exchanging designs among groups becomes much easier. Since intellectual property (IP) reuse is becoming a key factor in achieving rapid development of new products to meet time-to-market constraints, having an easy way to leverage on the IP portfolio is very important. Design reuse, especially in the case of soft IP, is greatly facilitated by the existence of a common design environment throughout a company. The design environment provides standard setup and initialization files, a common data structure for design data and technology data, a revision control mechanism, an easy way to select tool and design kit versions and several layers of software.

The standard setup and initialization files allow users to concentrate on the design. Since the system is integrated and has a standard configuration, most of the information needed to run tools can be pre-filled out, hence reducing the overhead for the users. Well-defined directory structures and naming conventions are the basis for a good design environment.

Revision control mechanisms are useful when the design is carried out by a large number of people. The usage model calls for a central repository, or *vault*, and individual work areas. The most common features provided by these systems are: (1) only one person at a time can access for edit a piece of design data (*check out with lock*); (2) a commented history of all the modifications for each cell is automatically maintained and can be accessed by any user; (3) as soon as a modified piece of data is *checked in* into the vault, it can be seen and used by any other person subscribed to that project.

Another important book-keeping mechanism for a project is to maintain a configuration file inside the project area to keep track of tool and DESIGN KIT versions used to do the specific design. This allows you to capture a snapshot of the environment for future comparisons between simulation data

and measurements, since the design system may have evolved after the design data was released for fabrication.

Software is developed to perform many different tasks within a design system: to add features which are not available by default in the off-the-shelf version of the tools; to post-process tools output data for presentation purposes or for use by a down-stream tool of the supported flow; to calculate derived parameters to be shown to designers; etc.

While providing all the default settings needed to use the DESIGN SYSTEM, the environment must be open in order to allow customization and accomodate the needs of expert users and other requirements. For example a specific project may need special versions of tools and/or design libraries; users may have preferences in the way their data is displayed, etc.

2.2 Design Kit

At the core of the DESIGN SYSTEM is the DESIGN KIT. This is a collection of objects that enable the designer to use a specific process. Hence, while all the other parts of the system are common for all processes, anything that is technology-specific is part of the DESIGN KIT.

A DESIGN KIT is composed of a technology library which contains all the primitive components available for a specific technology. Each component is fully characterized both electrically and physically. From the electrical point of view this means that models are available for all supported simulators. Nominal models are available as well as a number of corner cases to capture the statistical variation of process parameters. Both modeling and layout issues for low-power RF are topics of forthcoming sections(see sections 3 and 5). To make sure that the model being simulated corresponds to the structure that is going to be laid out, a set of routines are written to calculate the appropriate layout features of the cell, based upon the electrical values requested by the users. These same values are then passed to device generators that build the physical geometries using all the appropriate layers.

Finally, rule files for all the various layout verifications and for parasitic extraction provide the last piece of information necessary to close the loop before submitting the data for fabrication. Advanced LVS rules have been written to ensure not only that electrical equivalence is achieved, but also that the layout is realized exactly according to the parameters specified on the schematic. The reason for doing this is discussed in Section 3. Hence LVS checks must include verification of parameters like the number of fingers for multi-finger FETs, the presence of substrate contacts close to the devices, etc.

2.3 Design Methodology and Tool Flow

A Top-Down, Schematic-Driven Design Methodology is proposed in this DESIGN SYSTEM where all the information to drive simulators and layout generators is specified on the schematic. Figure 2 depicts the Design Flow.

At the top of the block diagram, the tool for capturing the design can be found. As we discussed in Section 2.1, the philosophy of having a common design environment calls for maintaining only one schematic capturing tool. The tool can then be integrated with a set of simulators which perform different types of simulations according to the application. Some of the simulators are tightly integrated with the schematic allowing the usage of the schematic itself to cross-probe the simulation results. RF simulation-specific issues are covered in great detail in Section 4.

Schematic and layout editors are tightly integrated through the usage of layout generators. Any component parameter can be changed at any time during the design process and the change can be propagated from the schematic view to the layout view and viceversa. Also, connectivity information is available in the layout tool, thus reducing almost to zero the probability of making mistakes in the

routing phase. The graphical information provided about connectivity helps during the placement phase as well. Other sophisticated tools developed in-house allow us to migrate designs from one technology to another, as described in Section 5.

The integration of layout and verification tools allow layout designers to quickly check the correctness of the layout interactively while working on it. All the checks are available through menu picks. Layout engineers can decide whether to use their local machine for small verification jobs or submit them to computer servers.

Once the layout is completed, several steps are required before the data is validated. First a Design Rule Checking is performed to ensure that the layout conforms to all manufacturing specifications. Then a Layout Versus Schematic check is run to ensure electrical equivalence between layout and schematic.

Finally, a parasitic extraction is performed and the whole circuit is re-simulated. If the circuit is too large, it may not be possible to simulate the whole thing at transistor level. In this case behavioral models can be written for less sensitive blocks and they can be used together with the extracted description of other blocks to carry out the simulation. With the advent of System on Chip, behavioral modeling is becoming more and more important for analog and RF devices.

3 Modeling for RF

One of the most important capabilities that a Design System has to provide is the transfer of accurate information about device performance from the silicon to the designer. Simulation results can only be as accurate as the models used to mathematically describe the physical behavior of the devices. Therefore, a very important part of a design system is the accuracy of the models. In this section we will analyze some of the issues encountered when modeling the behavior of some passive and active integrated components for RF applications.

3.1 MOS transistor

Digital applications have been the major driver for the development of the CMOS technology. As a consequence, most of the research efforts on MOS modeling have been focused towards digital design.

Advances in lithography allow us to build MOS devices with shorter channel lengths operating at lower voltages. As device geometries shrink to deep submicron dimensions, circuit performance is pushed to the limits of process capability and MOS transistors are used for high frequency applications in places where BJTs were previously the only viable candidates.

The main goal in digital design is to apply the principles of scaling to obtain higher switching speed and lower power dissipation [2]. In addition to these performance requirements, RFIC designers have to deal with other issues like noise, gain, linearity and efficiency.

Throughout the years MOSFET models have evolved from very simple physics-based analytical models (e.g. spice level 1,2,3) [3] to more empirical ones (e.g. BSIM2, Hspice level 28) with many non-physical parameters to better fit measurement data. However, recently introduced models are based on more advanced device physics and have physically-meaningful model parameters, e.g. Phillips MOS 9, BSIM3v3 [4, 5] and EKV [6, 7]. Originally, most of the model development was done to achieve a good fit for DC characteristics while the main requirement for the capacitance model was good continuity rather than good fit. The new frequency regimes, in which MOS transistors are now employed, put more demand on the accuracy of the AC part of the MOSFET model in addition to the DC one, both requiring careful validation of the extracted model parameters. Although BSIM3v3 is the *de facto* public-domain industry standard MOS model, it has limitations when approaching a few GHz, giving

inaccurate results. The same is true for all the compact models currently available, which need to be enhanced to predict correct RF behavior. In order to do that, the modeling expert is presented with two choices:(1) develop new compact models and ask tool vendors to implement them within their simulators; (2) develop composite models, augmenting existing models to extend their capabilities. From a DESIGN SYSTEM perspective it is better to keep the intrinsic model standard so that it would be available in all simulators, and then add extra components to achieve a better agreement with measurements. To check for the validity of the high-frequency portion of the composite model, S-parameter measurements are used.

The main effects that need to be accounted for and that are not present in standard MOS models are:

- Terminal resistances, in particular the gate, both for their resistive and noise contributions;
- Signal coupling through the substrate within the device and between devices;

In Figure 3 the cross-section of the MOS transistor and all its parasitic components are shown [8]. Drain and source diodes are pulled out of the intrinsic model in order to have access to the internal drain and source nodes. A comprehensive treatment on the subject of MOS Modeling with thorough analyses of the latest models can be found in [9].

Figure 3 also shows a compact scaleable model that has been derived and implemented for SPICE simulation as described in [8, 10]. This model is based on the quasi-static approximation and it was found to provide simulation results in good agreement with measurements up to about $10GHz$ [8].

Using this simple equivalent circuit has several advantages over more complicated ones that take Non-Quasi-Static effects into account. First of all, simulation time is not compromised since only a few nodes are added; second, a simplified set of equations can be derived from it to analytically relate the values of the extrinsic and intrinsic components with the Y-parameters.

$$y_{11} = \frac{j\omega C_{gg}}{1 + j\omega R_g C_{gg}} \tag{1}$$

$$y_{12} = \frac{-j\omega C_{gd}}{1 + j\omega R_g C_{gg}} \tag{2}$$

$$y_{21} = \frac{g_m - j\omega(C_m + C_{gd})}{1 + j\omega R_g C_{gg}} \tag{3}$$

$$y_{22} = \frac{g_{ds} + j\omega(C_{db} + C_{gd})}{1 + j\omega R_g C_{gg}} \tag{4}$$

where C_{gg} represents the total gate capacitance, R_g the gate resistance, C_{gd} the total gate-to-drain capacitance, C_{db} the total drain-to-bulk capacitance, C_m the transcapacitance that represents the nonreciprocal capacitance effect between gate and drain, g_m the transconductance and g_{ds} the output conductance.

S-parameter measurements carried out on the MOS transistor biased in its linear region of operation are then used for a direct extraction of the RF model parameters, as presented in [8]. Finally, de-embedding techniques are applied to separate the device contributions from the ones due to the measurement setup and surrounding environment [11].

The care with which RF device models are extracted suggests that every parameter is highly critical and that to get good agreement between simulated and manufactured devices,

To achieve good agreement between simulated and measured devices, the RF model must be extracted with great care and the design system must be very well controlled. Consider the case of sizing a MOSFET: W and L alone are not enough to fully characterize the electrical behavior of your

device. You also need to know the number of fingers used for the gate, the location of the substrate contacts, etc. It is clear from the measurements that all of these parameters greatly affect the device performance [10]. Consider the example of a MOS transistor laid out with an even number of fingers and one for which an odd number of fingers has been used. Figure 4 shows the difference between these two devices. Although the total width and length are the same for the two devices, area and perimeters of drain and source differ in the two configurations. This can be a desired effect: designers can assign a bigger area to the source when it is connected to ground, for example. By doing this they can obtain a higher driving current without increasing the drain-to-bulk parasitic capacitance. This yields two considerations: first, the device is no longer symmetrical, but one of the two terminals has more diffusion-to-bulk parasitics associated with it; second, the intra-device substrate resistive paths from diffusion to the bulk contacts are different in the two cases. The model needs to be aware of this difference in order to correctly predict the device behavior.

Another important aspect of the transistor model is to accurately predict the noise behavior. As it will be made clear later, there is a direct relationship between power dissipation and noise in RF design. Hence, the more accurate the noise prediction, the less over-design is necessary. There are many sources of noise within a MOS transistor: noise at the drain due to both channel thermal noise and flicker noise; thermal noise due to the terminal resistances and to substrate resistance, see [10].

3.2 Bipolar

The bipolar junction transistor (BJT) is still dominates the RFIC domain. It has better performance than the MOSFET and has a significantly lower cost than $GaAs$ devices. Moreover, at a moderate cost penalty, it can be integrated together with standard CMOS into a BiCMOS process, making it very attractive for System on Chip applications. While MOS applications are starting to go beyond the many hundreds of MHz up into the few GHz range, the bipolar transistor is moving into the tens of GHz to replace the expensive $GaAs$ technology. Also, $SiGe$ bipolar technologies are receiving more attention, since they allow a significantly higher f_t with a small increase in costs.

Because of the drive from the digital industry on CMOS modeling, bipolar transistors have received less attention. The standard model is still the Spice Gummel-Poon Model (SGPM). New models have been developed in the past 10-15 years and are now being evaluated by the Compact Model Council to replace Gummel-Poon as the new public-domain industry standard. One of the candidates is Hicum. This model was first introduced in [12, 13]. It has been further developed within Conexant and the latest results can be found in [14]. This model is more accurate than SGPM in particular regions of operation but designers have to trade-off accuracy with simulation speed. Both SGPM and Hicum are available in our Design Kit, leaving the designer to choose which one is better suited for the specific application.

Parameter extraction strategies are very important for bipolar models. Typically, parameter extraction for bipolar transistors is carried out using a single-transistor fitting strategy. This approach has several limitations: it relies on "golden" wafers which are hard to obtain; it often results in unrealistic/non-physical parameter values; it can only produce a simple equivalent circuit without any geometry-related information; it can be used for a library with a limited number of devices, unless time and resources are unlimited.

A parameter extraction methodology, targeting scaleable and predictive modeling has been developed. This methodology allows one to derive model parameters for a wide variety of device configurations, using the measurement of a subset of these configurations strategically located within the device space as data points. This methodology has several advantages: it enables extraction of an accurate physics-based equivalent circuit with a realistic representation of parasitic components; the extracted

parameters have a physical meaning, hence they can be changed if process shifts occur, without having to re-extract them; it allows one to generate models for many different transistor configurations with a minimum number of measurements.

3.3 Passive Devices

All passive devices need to be accurately modeled for RF applications. In most cases the first-order models cannot be used. In particular, if these devices are used to build on-chip impedance-matching networks, the effect of parasitic capacitance to substrate and of the lossy substrate have to be added in order to achieve good agreement with S-parameter measurement.

3.3.1 Monolithic Spiral Inductors

Planar inductors have been used for many years in circuits with insulating or semi-insulating substrates. In the early development of silicon integrated circuits (Si IC's), planar inductors were investigated [15], but large chip areas due to lithography limitations, low Q's and low-frequencies of operation lead to the conclusion that integrating inductors on chip was impractical. At the beginning of the '90s Nguyen and Meyer demonstrated that it was possible to make usable inductors on Si IC's [16, 17].

Monolithic spiral inductors are now widely used in RF designs. With inductance values ranging from $1nH$ to about $6nH$, these components can be effectively used both for impedance matching and as collector loads [18]. For low voltage operation, not only do inductor loads provide impedance matching, but they also allow for voltage swing above positive supply.

The monolithic spiral inductor is by far the most challenging passive component to model with a compact model. A lot of research efforts have been devoted lately to this objective. Interesting results can be found in [19]. To support the design using spiral inductors, scaleable models with associated parasitics and substrate loss terms were developed based on electromagnetic simulation and lab measurement results. In addition, a parametric utility was derived and integrated into the DESIGN SYSTEM to calculate physical geometries for specified values.

3.4 Package Modeling

Low-cost packaging is essential for moderate and high volume commercial wireless products. In some cases more expensive multi-die packages and/or multi-chip modules (MCM) may be required to reduce parasitics between circuits that need to be on separate die but perform strictly interconnected functions. In both cases it is essential to quantify the effects that package parasitics will have on the circuit being designed. For this reason accurate electrical models for the package and for the network of bondwires that connect the die to the package are derived utilizing electromagnetic simulation in conjunction with measurements to verify and fine tune the resulting model. These fully-coupled, lumped-element models can then be used to carry out SPICE simulations.

Knowing the parasitics for a particular package, it is possible to design the layout to minimize the detrimental effects and even to take advantage of these parasitics. For example, to reduce crosstalk between signal leads, it is common practice to assign one or more ground leads between the signals. To lower ground inductance, it is also common to assign multiple leads to ground and in some cases to use the package die attach paddle as a ground plane. Finally, for impedance matching applications, designers can utilize bondwire or package lead parasitics in the design of matching networks to save on internal and external components.

4 Simulation for Low-Power RF Circuits

In RF systems power trades off against noise, linearity, and bandwidth performance [33]. In order to implement a minimum power design one must be able to accurately verify its performance. Any uncertainty in your ability to verify the performance requires an equal amount of overdesign, and overdesign requires more power. In particular, one must be able to accurately verify the performance in terms of noise, linearity, and speed, because these are the primary factors that determine how much power is required in RF circuits. Accurate simulation is a critical prerequisite for minimum-power design.

4.1 Characteristics of RF Circuits

RF circuits have many unique characteristics that make them difficult to verify with SPICE. Lately new RF simulators based on harmonic balance and shooting methods have become available that overcome these obstacles [26].

4.1.1 High-Frequency Carriers

The basic purpose of the RF section of a transmitter is to translate the baseband information signal to the allotted frequency band and inject it into the channel. This is done by using the information signal to modulate a high frequency carrier signal. In the receiver the RF section extracts the desired signal from the channel and translates it back down to baseband by demodulating, or stripping the carrier, from the input signal. In both cases, the RF sections are processing modulated carriers.

Modulated carriers are characterized as having a periodic high-frequency carrier signal and a low-frequency modulation signal that acts on either the amplitude, phase, or frequency of the carrier. For example, a typical cellular telephone transmission has a 10-30 kHz modulation bandwidth riding on a 1-2 GHz carrier. When simulating modulated carriers, SPICE must use small timesteps to follow the high frequency carrier and must simulate for a long time to represent the low frequency modulation. Thus, the simulations can be overwhelmingly expensive because of the large number of timesteps needed. The primary goal of RF simulation is to efficiently simulate circuits that must be accurately simulated over these two widely separated time scales.

4.1.2 Linear Time-Varying Nature of the RF Signal Path

RF circuits are designed to be as linear as possible from input to output to prevent distortion of the modulation or information signal. Some circuits, such as mixers, are designed to translate signals from one frequency to another. To do so, they are driven by an additional signal, the local oscillator (LO), a large periodic signal whose frequency equals the amount of frequency translation desired. For best performance, mixers are designed to respond in a strongly nonlinear fashion to the LO. Thus, mixers behave both near-linearly (to the input) and strongly nonlinearly (to the LO).

The LO signal is a periodic signal with a constant amplitude and frequency. It is independent of the information signal, and so may be considered to be part of the circuit rather than an input to the circuit as shown in Figure 5. This simple change of perspective allows the mixer to be treated as having a single input and a near-linear, though periodically time-varying, transfer function.

SPICE provides the small-signal AC and noise analyses, that are considered essential when analyzing amplifiers and filters. Small-signal analyses predict the response of the circuit when the circuit stimulus is infinitesimal. However, they do so by linearizing a nonlinear time-invariant circuit about a constant operating point, and so generate a linear time-invariant (LTI) representation. An LTI system cannot

exhibit frequency translation, thus this approach cannot be used to predict the performance of most RF circuits such as mixers and oscillators, where frequency translation is a critical aspect of their behavior. Linearizing a nonlinear circuit about a periodically-varying operating point extends small-signal analysis so that it can handle these types of circuits.

All of the traditional small-signal analyses can be extended in this manner, enabling a wide variety of applications. In particular, a noise analysis that accounts for cyclostationary noise [32] can be implemented that fills a critically important need for RF circuits.

4.2 RF Analyses

Spice provides several different types of analyses that have proven themselves essential to designers of baseband circuits. These same analyses are also needed by RF designers, except they must be extended to address the issues described in the previous section. The basic Spice analyses include DC, AC, noise, and transient. RF versions of each have been developed in recent years based on two different foundations, harmonic balance and shooting methods. Both harmonic balance and shooting methods started off as methods for computing the periodic steady-state solution of a circuit, but have been generalized to provide all the functionality needed by RF designers. Harmonic balance and shooting method simulation algorithms have progressed to the point where both provide roughly the same level of capabilities.

4.2.1 Periodic and Quasiperiodic Analysis

Periodic and quasiperiodic analyses can be thought of as RF extensions of Spice's DC analysis. In DC analysis one applies constant signals to the circuit and it computes the steady-state solution, which is the DC operating point about which subsequent small-signal analyses are performed. Sometimes, the level of one of the input signals is swept over a range and the DC analysis is used to determine the large-signal DC transfer curves of the circuit.

With periodic and quasiperiodic analyses, the circuit is driven with one or more periodic waveforms and the steady-state response is computed. This solution point is used as a periodic or quasiperiodic operating point for subsequent small-signal analyses. In addition, the level of one of the input signals may be swept over a range to determine the power transfer curves of the circuit.

Periodic and quasiperiodic analyses are generally used to predict the distortion of RF circuits and to compute the operating point about which small-signal analyses are performed (presented later). When applied to oscillators, periodic analysis is used to predict the operating frequency and power, and can also be used to determine how changes in the load affect these characteristics (load pull).

Quasiperiodic steady-state (QPSS) analyses compute the steady-state response of a circuit driven by one or more large periodic signals. The steady-state or eventual response is the one that results after any transient effects have dissipated. Such circuits respond in steady-state with signals that have a discrete spectrum with frequency components at the drive frequencies, at their harmonics, and at the sum and difference frequencies of the drive frequencies and their harmonics. Such signals are called quasiperiodic and can be represented with a generalized Fourier series

$$v(t) = \sum_{k=-\infty}^{\infty} \sum_{\ell=-\infty}^{\infty} V_{k\ell} e^{\jmath\pi(kf_1+\ell f_2)t} \tag{5}$$

where $V_{k\ell}$ are Fourier coefficients and f_1 and f_2 are fundamental frequencies. For simplicity, a 2-fundamental quasiperiodic waveform is shown in (5), though quasiperiodic signals can have any finite number of fundamental frequencies. If there is only one fundamental, the waveform is simply periodic.

f_1 and f_2 are assumed to be noncommensurate, which means that there exists no frequency f_0 such that both f_1 and f_2 are exact integer multiples of f_0. If f_1 and f_2 are commensurate, then $v(t)$ is simply periodic.

The choice of the fundamental frequencies is not unique. Consider a down-conversion mixer that is driven with two periodic signals at f_{RF} and f_{LO}, with the desired output at $f_{\mathrm{IF}} = f_{\mathrm{RF}} - f_{\mathrm{LO}}$. The circuit responds with a 2-fundamental quasiperiodic steady-state response where the fundamental frequencies can be f_{RF} and f_{LO}, f_{LO} and f_{IF}, or f_{IF} and f_{RF}. Typically, the drive frequencies are taken to be the fundamentals, which in this case are f_{RF} and f_{LO}, With an up-conversion mixer the fundamentals would likely be chosen to be f_{IF} and f_{LO}.

As discussed in Section 4.1.2, computing signals that have the form of (5) with traditional transient analysis would be very expensive if f_1 and f_2 are widely spaced so that $\min(f_1, f_2)/\max(f_1, f_2) \ll 1$ or if they are closely spaced so that $\min(f_1, f_2)/\max(f_1, f_2) \ll 1$. Large-signal steady-state analyses directly compute the quasiperiodic solution without having to simulate through long time constants or long beat tones (the beat tone is the lowest frequency present excluding DC). The methods generally work by directly computing the Fourier coefficients, $V_{k\ell}$. To make the computation tractable, it is necessary for all but a small number of Fourier coefficients to be negligible. These coefficients would be ignored. Generally, we can assume that all but the first K_i harmonics and associated cross terms of each fundamental i are negligible. With this assumption, $K = \prod_i (2K_i + 1)$ coefficients remain to be calculated, which is still a large number if the number of fundamentals is large. In practice, these methods are typically limited to a maximum of 3 or 4 fundamental frequencies.

Versions of periodic and quasiperiodic steady-state analyses exist for both harmonic balance and shooting methods [25].

4.2.2 Small-Signal Analyses

The AC and noise analyses in Spice are referred to as small-signal analyses. They assume that a small signal is applied to a circuit that is otherwise at its DC operating point. Since the input signal is small, the response can be computed by linearizing the circuit about its DC operating point (apply a Taylor series expansion about the DC equilibrium point and discard all but the first-order term). Superposition holds, so the response at each frequency can be computed independently. Such analyses are useful for computing the characteristics of circuits that are expected to respond in a near-linear fashion to an input signal and that operate about a DC operating point. This describes most "linear" amplifiers and continuous-time filters.

The assumption that the circuit operates about a DC operating point makes these analyses unsuitable for circuits that are expected to respond in a near-linear fashion to an input signal but that require some type of clock signal to operate. Mixers fit this description, and if one considers noise to be the input, oscillators also fit. However, there is a wide variety of other circuits for which these assumptions also apply. Circuits such as samplers and sample-and-holds, switched-capacitor and switched-current filters, chopper-stabilized and parametric amplifiers, frequency multipliers and dividers, and phase detectors. These circuits, which are referred to as a group as clocked circuits, require the traditional small-signal analyses to be extended such that the circuit is linearized about a periodically-varying operating point. Such analyses are referred to as linear periodically-varying or LPV analyses.

A great deal of useful information can be acquired by performing a small-signal analysis about the time-varying operating point of the circuit. LPV analyses start by performing a periodic analysis to compute the periodic operating point with only the large clock signal applied (the LO, the clock, the carrier, etc.). The circuit is then linearized about this time-varying operating point (expand about the periodic equilibrium point with a Taylor series and discard all but the first-order term) and the small information signal is applied. The response is calculated using linear time-varying analysis. Consider a

circuit whose input is the sum of two periodic signals, $u(t) = u_{\rm L}(t) + u_{\rm s}(t)$, where $u_{\rm L}(t)$ is an arbitrary periodic waveform with period $T_{\rm L}$ and $u_{\rm s}(t)$ is a sinusoidal waveform of frequency $f_{\rm s}$ whose amplitude is small. In this case, $u_{\rm L}(t)$ represents the large clock signal and $u_{\rm s}(t)$ represents the small information signal.

Let $v_{\rm L}(t)$ be the steady-state solution waveform when $u_{\rm s}(t)$ is zero. Then allow $u_{\rm s}(t)$ to be nonzero but small. We can consider the new solution $v(t)$ to be a perturbation $v_{\rm s}(t)$ on $v_{\rm L}(t)$, as in $v(t) = v_{\rm L}(t) + v_{\rm s}(t)$. The small-signal solution $v_{\rm s}(t)$ is computed by linearizing the circuit about $v_{\rm L}(t)$, applying $u_{\rm s}(t)$, and then finding the steady-state solution.

$$u_{\rm s} = U_{\rm s} e^{j2\pi f_{\rm s} t} \tag{6}$$

Given that perturbation, in steady-state the response is given by

$$v_{\rm s} = \sum_{k=-\infty}^{\infty} V_{{\rm s}k} e^{j2\pi(f_{\rm s} + k f_{\rm L})t} \tag{7}$$

where $f_{\rm L} = 1/T_{\rm L}$ is the large signal fundamental frequency. $V_{{\rm s}k}$ represents the sideband for the $k^{\rm th}$ harmonic of $V_{\rm L}$. In this situation, shown in Figure 6, there is only one sideband per harmonic because $U_{\rm s}$ is a single frequency complex exponential and the circuit has been linearized. This representation has terms at negative frequencies. If these terms are mapped to positive frequencies, then the sidebands with $k < 0$ become lower sidebands of the harmonics of $v_{\rm L}$ and those with $k > 0$ become upper sidebands.

$V_{{\rm s}k}/U_{\rm s}$ is the transfer function for the input at $f_{\rm s}$ to the output at $f_{\rm s} + k f_{\rm L}$. Notice that with periodically-varying linear systems there are an infinite number of transfer functions between any particular input and output. Each represents a different frequency translation.

Versions of this type of small-signal analysis exists for both harmonic balance [27] and shooting methods [29, 30].

There are two different ways of formulating a small-signal analysis that computes transfer functions. The first is akin to traditional AC analysis, and is referred to here as a "periodic AC" or PAC analysis. In this case, a small-signal is applied to a particular point in the circuit at a particular frequency, and the response at all points in the circuit and at all frequencies is computed. Thus, in one step one can compute the transfer function from one input to any output. It is also possible to do the reverse, compute the transfer functions from any input to a single output in one step using an 'adjoint' analysis. This is referred to as a "periodic transfer function" or PXF analysis. PAC is useful for predicting the output sidebands produced by a particular input signal, whereas PXF is best at predicting the input images for a particular output [35].

Small-signal analysis is also used to perform cyclostationary noise analysis [21, 30, 34], which is an extremely important capability for RF designers. It is referred to as a "periodic noise" or PNoise analysis, and is used to predict the noise figure of mixers. PNoise analysis is also used to predict the phase noise of oscillators, however this is a numerically ill-conditioned problem that requires special techniques in order to overcome the ill-conditioning and accurately compute close-in phase noise [24].

LPV analyses provides significant advantages over trying to get the same information from equivalent large signal analyses. First, they can be much faster. Second, a wider variety of analyses are available. For example, noise analysis is much easier to implement as a small-signal analysis. Finally, they can be more accurate if the small signals are very small relative to the large signals. Small signals applied in a large signal analysis can be overwhelmed by errors that stem from the large signals. In a small-signal analysis, the large and small signals are applied in different phases of the analysis. Small errors in the large signal phase typically have only a minor effect on the linearization and hence the accuracy of the small-signal results.

All of the small-signal analyses are extensible to the case where the operating point is quasiperiodic. This is important when predicting the effect of large interferers or blockers. Such analyses are referred to as linear quasiperiodically-varying or LQPV analyses as a group, or individually as QPAC, QPXF, QPNoise, etc.

4.2.3 Transient-Envelope Analyses

Transient-envelope analyses are applied to simulate modulated carrier systems when the modulation waveform is something other than a simple sinusoid or combination of sinusoids. It does so by performing a series of linked large-signal pseudo-periodic analyses, which are periodic analyses that have been modified to account for slow variations in the envelope over the course of each period of the carrier as a result of the modulation. The pseudo-periodic analyses must be performed often enough to follow the changes in the envelope. In effect, transient-envelope methods wrap a conventional transient analysis algorithm around a modified version of a periodic analysis. Thus the time required for the analysis is roughly equal to the time for a single periodic analysis multiplied by the number of time points needed to represent the envelope. If the envelope changes slowly relative to the period of the carrier, then transient-envelope simulation can be very efficient relative to traditional transient analysis.

Transient-envelope methods have two primary applications. The first is predicting the response of a circuit when it is driven with a complicated digital modulation. An important problem is to determine the interchannel interference that results from intermodulation distortion. Simple intermodulation tests involving a small number of sinusoids as can be performed with quasiperiodic analysis are not a good indicator of how the nonlinearity of the circuit couples digitally modulated signals between adjacent channels. Instead, one must apply the digital modulation, simulate with transient-envelope methods, and then determine how the modulation spectrum spreads into adjacent channels.

The second important application of transient-envelope methods is to predict the long term transient behavior of certain RF circuits. Examples include the turn-on behavior of oscillators, power supply droop or thermal transients in power amplifiers, and the capture and lock behavior of phase-locked loops. Another important example is determining the turn-on and turn-off behavior of TDMA transmitters. TDMA (time-division multiple access) transmitters broadcast during a narrow slice of time. During that interval the transmitter must power up, stabilize, send the message, and then power down. If it powers up and down too slowly, the transmitter does not work properly. If it powers up and down too quickly, the resulting spectrum will be too wide to fit in the allotted channel. Simulating with traditional transient analysis would be prohibitively expensive because the time slice lasts on the order of 10-100 ms and the carrier frequency is typically at 1 GHz or greater.

Versions of transient-envelope analysis exists for both harmonic balance [28] and shooting methods [31].

5 RF Layout Generation

Generating the layout of high-performance RF circuits is a difficult and time-consuming task which has a considerable impact on circuit performance. The various parasitics which are introduced during layout design can introduce severe performance degradation. The parasitic elements associated with interconnect wires cause loading and coupling effects that degrade the frequency behavior and the noise performance of RF circuits. Device mismatch and thermal effects put a fundamental limit on the achievable accuracy of circuits. Since these parasitics are unavoidable, the main concern in RF layout is to control and predict the effects of the parasitics on circuit performance and to make sure that the circuit after layout still performs within its specifications. In our design system, predictable

circuit performance is achieved through the systematic use of a schematic driven layout methodology. augmented with layout automation tools wherever possible.

5.1 Schematic Driven Layout

Fig. 7 gives an overview of our layout tool flow. At the heart of the system is a schematic driven layout editor that uses instance attributes from the schematic and a library of procedural device generators to create the initial layout for the circuit. The tool also extracts the connectivity from the schematic and uses it to drive subsequent interactive and automatic layout optimization steps.

The advantages of this schematic driven layout methodology are twofold. First, the use of procedural device generators and connectivity-driven editing style results in 5 to 7x productivity gain compared with manual polygon-level layout. The resulting circuit layout is correct by construction, which reduces the time spent in verification of the design.

The second advantage is tight control over the parasitic elements associated with the layout of devices. Examples of such parasitics are the series resistances and capacitances associated with MOS source and drain junctions and the parasitic components of resistors and capacitors. The values of these parasitic components are layout dependent and for high-performance analog and RF designs, their effect has to be taken into account throughout the design cycle. The use of procedural device generators results in predictable layout and hence predictable device parasitics. This allows to make accurate predictions of circuit performance early in the design cycle, before the actual layout is done.

5.2 Device Generators

An important component of our design system is the library of device generators. A device generator is a program that procedurally generates a layout for a device, based on a set of device parameters, a technology specification and a number of user specified options. In general, layouts created by device generators can be of any complexity, ranging from basic devices (transistors, capacitors, resistors) to complete amplifier stages. Virtually all of the commonly used analog-specific layout optimizations, e.g. device merging, layout symmetries and matching considerations, can be programmed into these generators. Writing and maintaining a library of module generators is a major engineering challenge and generator libraries turn out to be large software systems. It is therefore crucial that module generators are written in a process-independent way, to make it easy to port them to new technologies.

Fig. 8 illustrates how layout optimizations can be built into a device generator. The layout shown in the figure consists of two MOS transistors connected source to drain in a cascode configuration. No contacts are necessary on the diffusion regions that form the shared source/drain of the devices. This allows to put the poly gate wires at minimum distance, which results in substantially reduced parasitic source/drain capacitance on this node. The circuit designer can enforce the use of this layout style by instantiating the corresponding symbol in his schematic.

5.3 Analog Layout Automation

To enhance the productivity of layout designers, our system supports the interactive use of placement, routing and compaction tools. For successful automation of analog and RF layout, advanced place and route tools that can handle analog layout constraints such as symmetry and matching are required. As shown in Fig 7, a constraint editor is used to annotate these critical layout constraints to the schematic. Constraint-driven layout tools are used to enforce these constraints throughout the layout process. The reader is referred to [36, 38, 39] for an overview of academic approaches to automated analog layout

generation. Commercial tools that are based on these research efforts are starting to become available and they are used in our design system wherever possible.

5.4 Template Driven Layout

IP reuse is one of the key factors in achieving the engineering quality and the timely completion of today's complex RF designs. The hard IP reuse techniques that are emerging in digital design are hard to apply to RF building blocks, since these circuits have to be optimized for each application. All though RF and analog circuit topologies are frequently reused, the parameters of the individual devices are usually optimized to maximize the performance and to minimize the power consumption for a given specification. In practice, this means that a significant portion of the layout has to be redone each time a circuit topology is reused, and that a major portion of the benefit is lost.

To overcome this problem, we have developed a template driven layout technique that allows to reuse the layout of an analog circuit for different designs and/or process technologies. Our approach uses a layout template to capture an expert's knowledge of analog layout for a given circuit topology. The template is created once by an expert layout designer and captures his knowledge of analog specific constraints like symmetry, device matching and parasitic minimization. To generate a circuit layout for a new design, the designer supplies a schematic with the new device parameters for the circuit and/or a new technology file. The layout is generated by transforming the template into an actual layout using specialized analog shape optimization and compaction techniques. During this process, all the layout knowledge implemented in the template is preserved: the new layout has the same relative device configurations, the same wire trajectories and material types and the symmetry and matching relations as the template layout.

Figure 9 gives an overview of our template driven layout system. The input to the system consists of a template layout, a schematic with the new device sizes and a new process technology file. As a first step, a library of device generators is used to generate device layouts for the new device sizes specified in the schematic. The best layout variant for each device is selected during an optional shape optimization step. The shape optimizer is based on a novel algorithm that allows to optimize the shapes of individual devices while preserving the relative device configurations of the layout template [37]. Different aspect-ratio's of devices can be generated by varying the geometric parameters of the instances, e.g. changing the number of fingers of a transistor. As described in the previous section, this can affect the performance of the devices and therefore shape optimization is an optional step that is only applied for non-critical devices. After shape optimization, the original templates devices are replaced with the actual device layouts and a compaction tool is used to generate a new design rule correct layout that preserves all the analog constraints of the template. The compactor is an internally developed tool that was designed to support analog constraints like symmetry and matching. Another important feature of the tool is the capability to correctly resize wires based on their currents flowing through the circuit.

Figure 10 shows four layouts generated by our template driven layout system. Each layout implements the same differential amplifier circuit topology. The sizes of the transistors and passives of each amplifier are optimized for a given specification. The template driven layout tool described in this section allows a designer to generate these layouts in a couple of minutes.

6 Silicon-Aware Simulation: Pre and Post Layout

As we saw in Section 3, the way components are laid out directly influence their electrical behavior. Moreover, since the RF functions are integrated, the whole environment in which they operate should

be taken into account since the very early stages of the design. As we saw in Section 2 the DESIGN KIT contains all the technology information necessary to evaluate the actual sizes of the layout features of each component before the layout is even started. We then saw in Section 5 that these parameters are passed to the device generators which take care of laying out the device exactly the way the designer expects it to be. The next step for the designer is to estimate the parasitics due to the interconnects and take these also into account during the design phase. For this reason, special components have been derived by the designers and are available in the library. These components take as inputs the physical size of the estimated interconnect and then compute the electrical parameters that can be used for simulation. These models depend on the process parameters, so they need to be changed like any other primitive component when going from one technology to another.

Once the layout is completed and verified, it is ready to be extracted for the purpose of performing post-layout simulation. Because of the advanced LVS rules available in the DESIGN KIT, the extracted netlist has all the complex models for the technology devices that are available in the technology library. This makes the back-annotation possible since the netlist is identical to the initial one except for the presence of the parasitic components.

The type of extractions available in most commercial tools are: (1) lumped capacitance to ground, (2) coupled capacitance between nets, (3) distributed RC and (4) coupled distributed RC. Nowadays, mode (1) is mainly used for fast simulations of non-critical digital blocks, but even most of the digital designs need to go through coupled C or distributed RC to have a good understanding of the design performance. Anything below mode (3) and (4) is of little use for RFIC design, since the impact of the interconnect resistance is very important when dealing with narrow band blocks that need impedance matching to work properly. Unfortunately, at the moment there are no tools available that can extract the self-inductance and mutual inductance associated to interconnects. A lot of efforts are currently being devoted by both academia and industry to come up with methodologies and algorithms to extract interconnect inductances. The importance of these parasitic inductances is highlighted in Section 7.

One of the tools available within the system is a Hierarchy Editor. This tool allows the user to select the view to be used for the simulation of every sub-block of a design hierarchy. In this way the user can specify the blocks that should be simulated using the schematic view, the extracted view, etc. Even behavioral views can be specified. The Hierarchy Editor turns out to be a very useful tool for both pre- and post-layout simulation.

7 Design Examples

The design of two RFIC devices, which achieved first-pass silicon success using the DESIGN SYSTEM, is described. The devices are used in a Digital Spread Spectrum (DSS) Cordless Telephone operating in the 2.4GHz ISM band (2400MHz - 2483.5MHz): one device is a transceiver IC [32] containing a direct conversion receiver, direct up-conversion transmit mixer and a frequency synthesizer, the second device is a 20dBm power amplifier (PA) [33]. Both are manufactured in a 25GHz bipolar process. The new designs are based on 900MHz DSS ICs with similar functionality, the intention being to use the same baseband controller IC, with minimal ROM mask changes, for either frequency band. The RF sections of the two devices were redesigned to work at the higher frequency, the baseband circuits were largely unchanged and an extra prescaler circuit was added to the synthesizer, together with modifications to the division ratios to cover the new frequency range. The power amplifier was redesigned for use at 2.4GHz but in this case the topology was changed from single-ended to differential to reduce the sensitivity to packaging parasitics. Though the circuit functions were not new redesigning them for higher frequency operation is not without challenge and time to market pressures dictated a first-pass success which can only be accomplished with the use of a DESIGN SYSTEM with accurate models

and efficient RF simulation capabilities.

7.1 Top Level Schematic

A symbol for the top level of IC hierarchy and a package model symbol are placed on the top level simulation schematic along with external matching component and sources. The external components include modelling for self-resonant frequency (SRF) and equivalent series resistance (ESR) and some printed circuit board (PCB) trace parasitics and ground via inductance. It is highly desirable to make circuits as tolerant of PCB layout as possible so that a radio design can be quickly integrated into many different phone models. Including the circuit board and device package in circuit simulations is vital in obtaining first-pass silicon success.

7.2 Package Model

The 900Mhz DSS ICs use standard low-cost packaging (TQFP and TSSOP) but the suitability of such packaging at 2.4GHz was unknown at the start of the project. An MCM solution placing both die on one substrate was favoured as a less risky, though more expensive, solution. Time to market is a key factor, particularly in a new area like 2.4GHz DSS phones, so the added cost can be acceptable and reduced by subsequent redesign. MCM parasitics are dominated by the bond wires as there is no equivalent lead-frame and external components can be placed close to the die. Package models exist in the DESIGN SYSTEM for standard packages with defined lead-frames to which a model of the bonding can be added. The same model can be used for either package or MCM providing the model has some degree of customization - to remove unused pins or add down bonds to the low inductance die attach 'flag'. The main difference is the amount of self inductance, higher for a package to include lead frame and bond wire, and coupling coefficient dependent on the bond wire pitch. Values of self-inductance and coupling coefficient are characterized for different bond lengths and pitches. Multipliers were added to the package parasitic models so that circuit sensitivity to those parasitics could be examined in simulation.

Simulations of a single-ended PA design showed a difficulty in realizing an on-chip interstage match that required a collector load inductance of the same order of magnitude as a bond wire inductance. A differential design gets around this problem at the expense of a more complicated external radio design. A printed output match and power-combining network was designed for low cost and to obviate the need for low value, and low accuracy, chip capacitors. This approach is less suitable for inclusion on an MCM but simulations of the differential topology showed a low sensitivity to package parasitics and good confidence was obtained that performance in low cost packaging would be acceptable. A customized TSSOP20 package with four pins fused to the die attach paddle was used. Simulation results showed that power gain at 2.4GHz varied by less than +/- 0.5dB for a +/- 25% change in package self inductance and by +/- 0.5dB/-1dB for a +/- 25% change in mutual coupling. The package model is symmetrical about its long axis but imbalance in the differential signals was noted in simulation due the asymmetrical connection of power and ground bond wires. After this was identified, and the symmetry of the package model itself confirmed, the pin out was modified to improve the differential signal balance.

For the transceiver IC most circuits use a differential topology and packaging concerns lessened except for the LNA which is a single-ended common-emitter design. Parasitic inductance in series with the emitter will reduce high frequency gain and the receiver performance becomes sensitive to the package and board design. A TQFP package with the backside of the die attach paddle exposed was chosen to provide the lowest ground inductance for the LNA emitter. Floor bonds to the top surface

of the paddle were used and the exposed backside of the paddle soldered directly to the circuit board ground plane. This package was modelled by modifying the standard TQFP48. Both package models have mutual coupling six pins over on either side and the die attach paddle is modelled as a simple network of inductors with a single lumped capacitance to the PCB ground.

7.3 Trace Parasitic Modelling

Previous simulations of a 900MHz VCO showed a large discrepancy in tuning frequency compared to measurements. Parasitic inductance and capacitance in the VCO tank wiring accounted for the discrepancy. A simple first order trace parasitic model was created and used in subsequent designs including the 2.4GHz ICs discussed. The model is placed in simulation schematics to represent a piece of trace with an estimation of its size and geometry. The physical size (in microns) is passed into the model and the series resistance, series inductance and shunt capacitance to substrate are calculated. It is similar to many published spiral inductor equivalent circuits. The effect of the trace modelling can be seen in Figure 12 which shows the PA small signal frequency response both with and without trace parasitic modelling. Figure 12 also includes the measured small signal frequency response. The measured response is actually tuned slightly high in frequency; the peak gain lies between 2.5Ghz and 2.6GHz, because the sheet capacitance for that wafer was lower than the process nominal. The wafer sheet capacitance value was used for the comparative simulation results in figure 12 : 'Trace LRC' is the simulation result with predicted trace parasitics and 'No Trace' the case for no trace parasitics. The difference in peak gain frequency due to trace parasitics is approximately 300MHz which would certainly result in a miss-tuned design, and another silicon iteration, if not predicted in simulation. The use of trace parasitic models, as noted in Section 7, has the advantage that inductance can be included in simulations. For example 'RC only' in Figure 12 is a simulation including trace resistance and capacitance but no inductance. The exclusion of the trace inductance significantly modifies the circuit frequency response. Trace parasitic modelling for the PA design also highlighted the possibility of unnecessary I2R loss in low impedance circuits which was countered in layout floor-planning to keep those traces short. One disadvantage of using such parasitic models is that the simulation schematic may not be compatible with LVS unless the netlister can recognize and 'short' the trace symbols.

7.4 Design for Low Power

RFIC design for lowest power is a matter of optimizing many variables: at the highest architectural level the choice of frequency band, modulation scheme, transmit power and duty cycle will have a major bearing on power consumption. In the case of GSM, or CDMA, these are predefined by standards and even in the case of the DSS cordless phone example discussed here, the choice of unlicensed frequency bands is limited and operation in those bands is governed by some restriction. For a given system low power optimization involves the choice of IC technology, partitioning and the level of integration and often low-cost and small size must be part of the optimization. Advances in RFCMOS and BiCMOS technologies allow for very high levels of system integration and the possibility of trading increased digital circuit complexity for relaxed analog design. This opens another dimension for power reduction in RFIC design as digital circuit power dissipation reduces with process shrinks. At the circuit level accurate simulation is the key to design for the lowest power. Good package modelling and the inclusion of layout parasitics allow accurate prediction of gain and bandwidth (7.2 and 7.3). Figure 12 shows excellent agreement between simulation and measurement at 2.4GHz. Good device models with realistic process corners are desirable to minimise over-design to meet specification at process, temperature and supply voltage extremes. Good inductor prediction and modelling is important because inductance

value is as important as Q to maximize load impedance and, hence, gain. Increasing inductance values will limit bandwidth so the more accurate simulation is necessary. Standard SPICE small signal analysis is a quick and easy way to simulate gain and frequency response and assess circuit sensitivity to process, temperature and supply voltage variations and to parasitics. For the PA design, power gain was viewed in a small signal analysis using the equation: power = real (node voltage * conjugate (node current)). Voltage sources must be placed on the schematic at any nodes of interest, as ammeters, which may cause LVS problems if the netlister does not ignore them. Within the transceiver device circuits are voltage driven and signals were viewed directly. Accurate noise simulations are required meet signal-to-noise ratio specifications, or evaluate receiver noise figure, and requires the accurate gain and bandwidth simulations mandated above as well as accurate device noise models. For circuits that do not translate frequency SPICE small signal analysis works well but not for down conversion mixers where the extra capabilities of Periodic AC analysis (4.2.2) are necessary so that the mixer design can be optimized for low power. Noise is not such an issue for the transmit path because the signal levels are strong but transmit power, efficiency and linearity are extremely important for low power. Transmit power is the most dominant factor in the overall power consumption of a wireless system. How efficiently that transmit power is generated is a key focus. In the DSS Cordless Telephone binary phase-shift keying (BPSK) modulation is used which contains both amplitude and phase information thus there is a linearity requirement on the PA. Accurate large signal linearity prediction is necessary to optimize biasing for highest efficiency while meeting a linearity specification. Figure 11 shows the large signal gain compression characteristic for the 2.4GHz DSS PA comparing measured and simulated results for a sinusoidal signal at 2.5GHz. There is a small offset of less than 1dB in gain which may be due to some unaccounted losses in the measurement set-up (there is a similar offset in the small signal gain response shown in Figure 7). There is good agreement between the measured and simulated gain compression points. Linearity is often by the 1dB compression point and/or an IM3, which can be simulated using standard SPICE transient analysis. Ultimately it is of more interest to predict the output power and spectral spreading with BPSK modulation and use that analysis to optimize the transmit chain for lowest power such as Transient Envelope analysis (4.2.3).

8 Conclusion

An RF Design System has to provide the designer with everything necessary to accurately predict the behavior of RFIC devices, including layout and package parasitic effects. A well-defined and integrated system is needed to obtain a manufacturable design that meets specifications at minimum cost and in the minimum time. A close link between schematic, models and layout is of paramount importance to ensure the accuracy needed for RF design. In this paper, we gave an overview of the advanced methods and tools currently available for simulation and noise analysis and of RF devices. We described tools and methologies that can be used for automatic RF layout generation and migration. To demonstrate the effectiveness of our system, we discussed the design of two RFIC devices, which achieved first-pass silicon.

9 Acknowledgment

ACKNOWLEDGMENT – Paolo ==========

The authors would like to thank Bijan Bhattacharyya, Mishel Matloubian, Yuhua Cheng, Christian Enz, Michael Schröter, Tzung-Yin Lee, Jie Yu, Florin Balasa, Larry Edwards, Horn Hsieh, Paramjit Singh, Arya Raychaudhuri, Rajesh Divecha, for fruitful and interesting discussions and also all the

teams within the Design Automation organization of Conexant who have contributed to the realization of this Design System.

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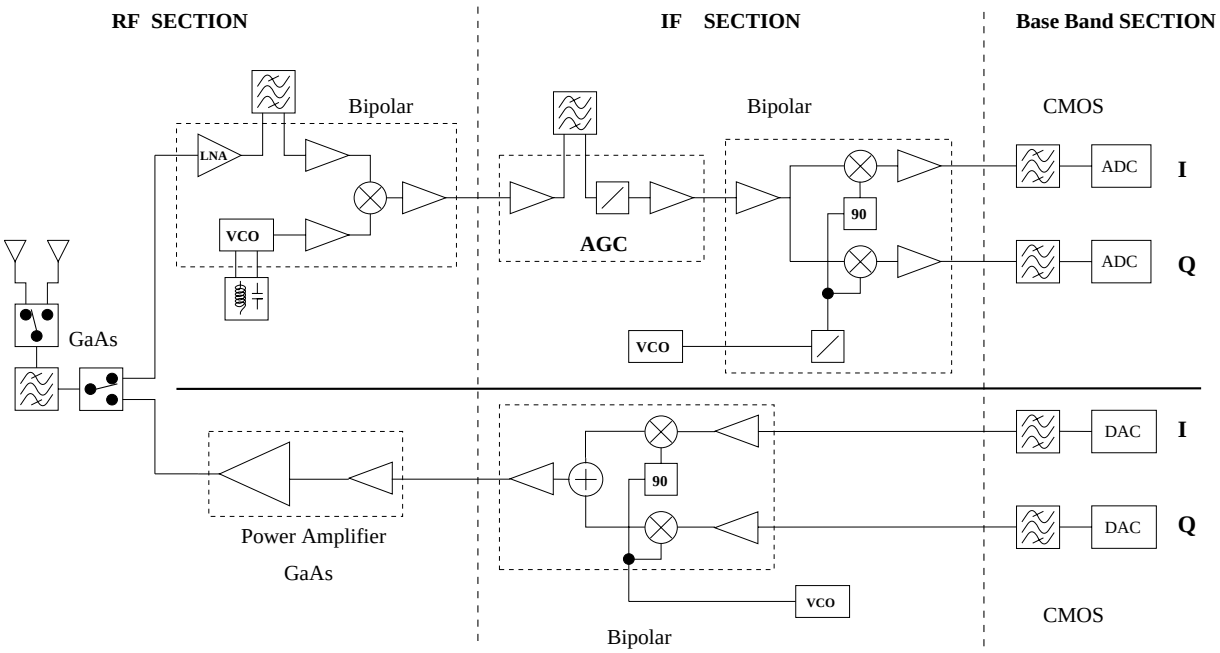

Figure 1: Example of a Super-Heterodyne Transceiver implemented using multiple technologies (Courtesy of P. Gray, UC Berkeley, ISSCC97)

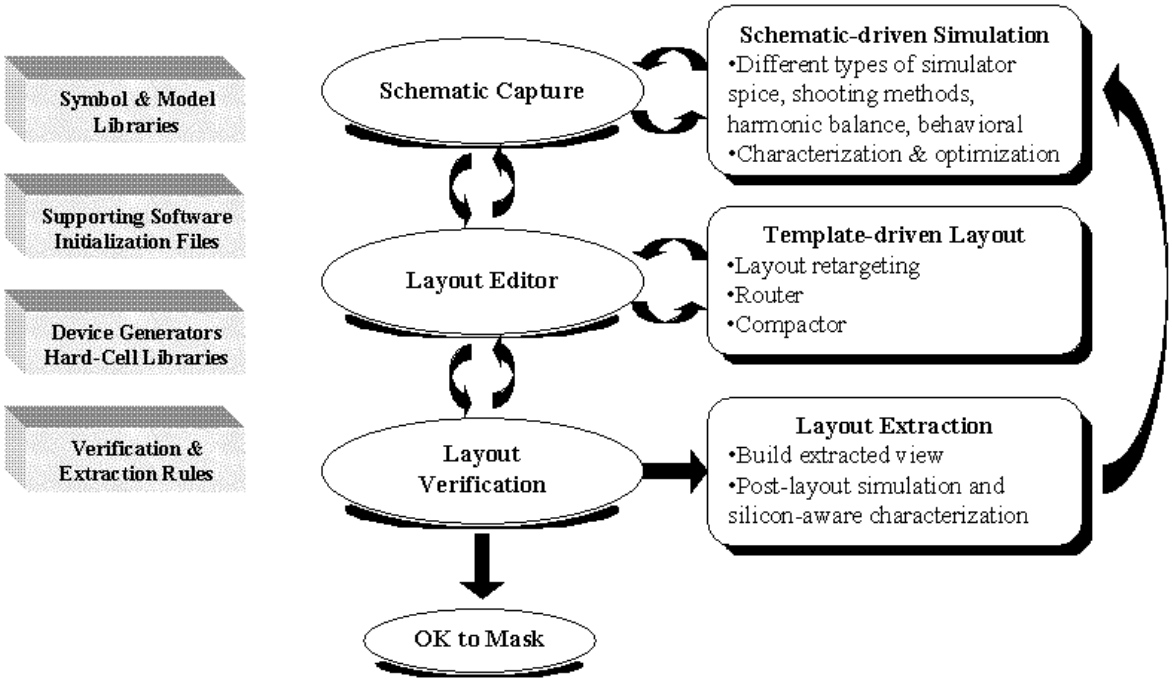

Figure 2: RFIC Design Methodology and Tool Flow

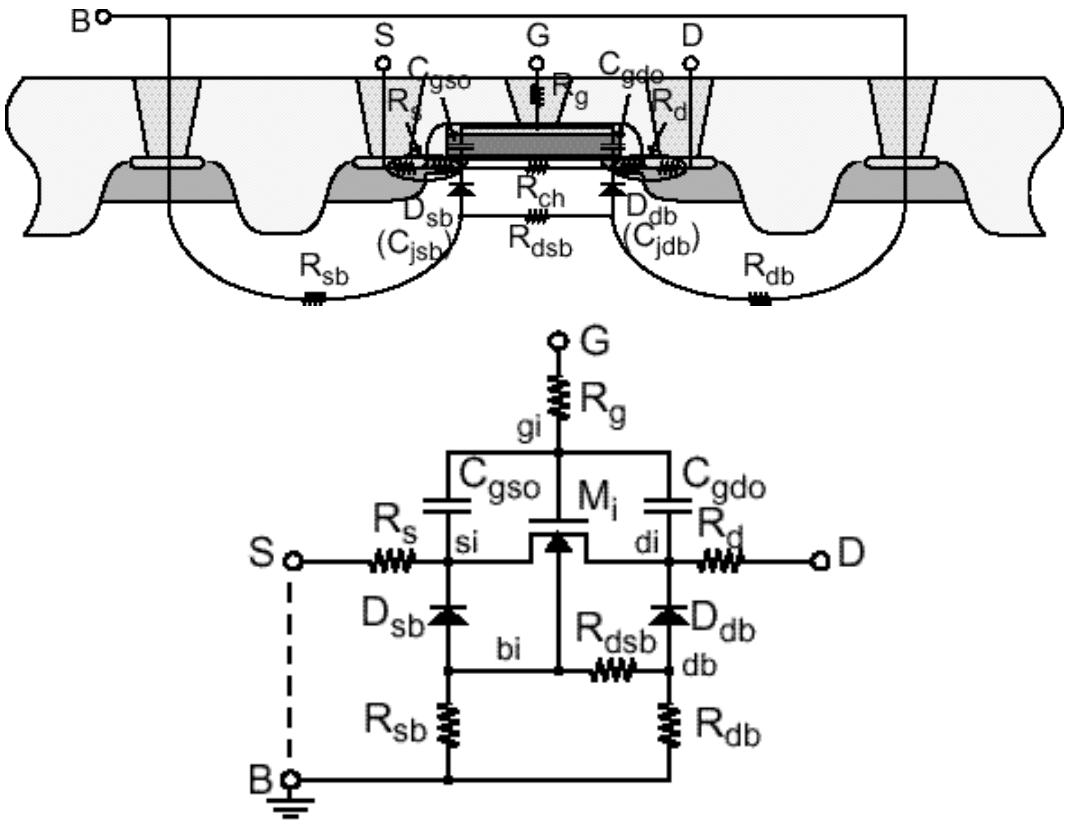

Figure 3: Cross-section and derived composite model of the RF MOS transistor

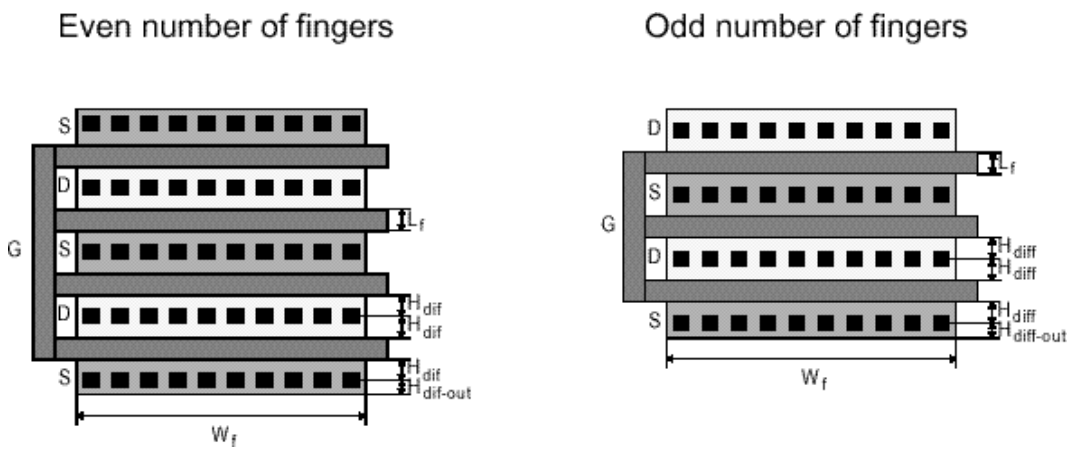

Figure 4: Layout of a MOS transistor with an even and a odd number of fingers

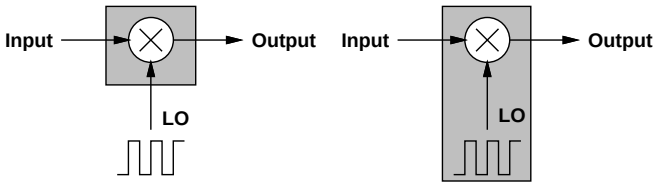

Figure 5: Instead of thinking of a mixer as a circuit with two inputs (left), one of which is the LO, one can conceptually think of the LO as being part of the mixer (right). In this case the mixer has a single input and responds in a near-linear, but time-varying, manner to the input signal.

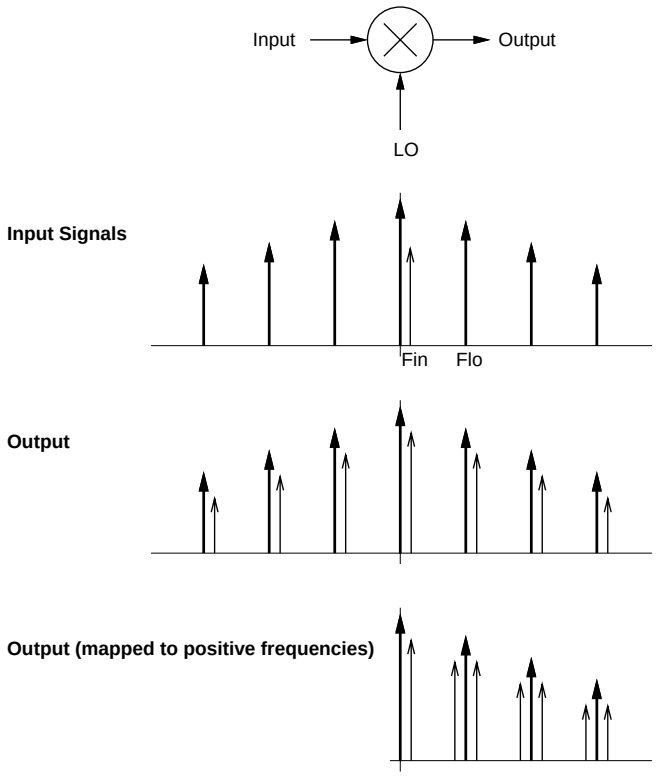

Figure 6: The steady-state response of a linear periodically-varying system to a small complex exponential stimulus. The large signals are represented with solid arrows and the small signals with hollow arrows.

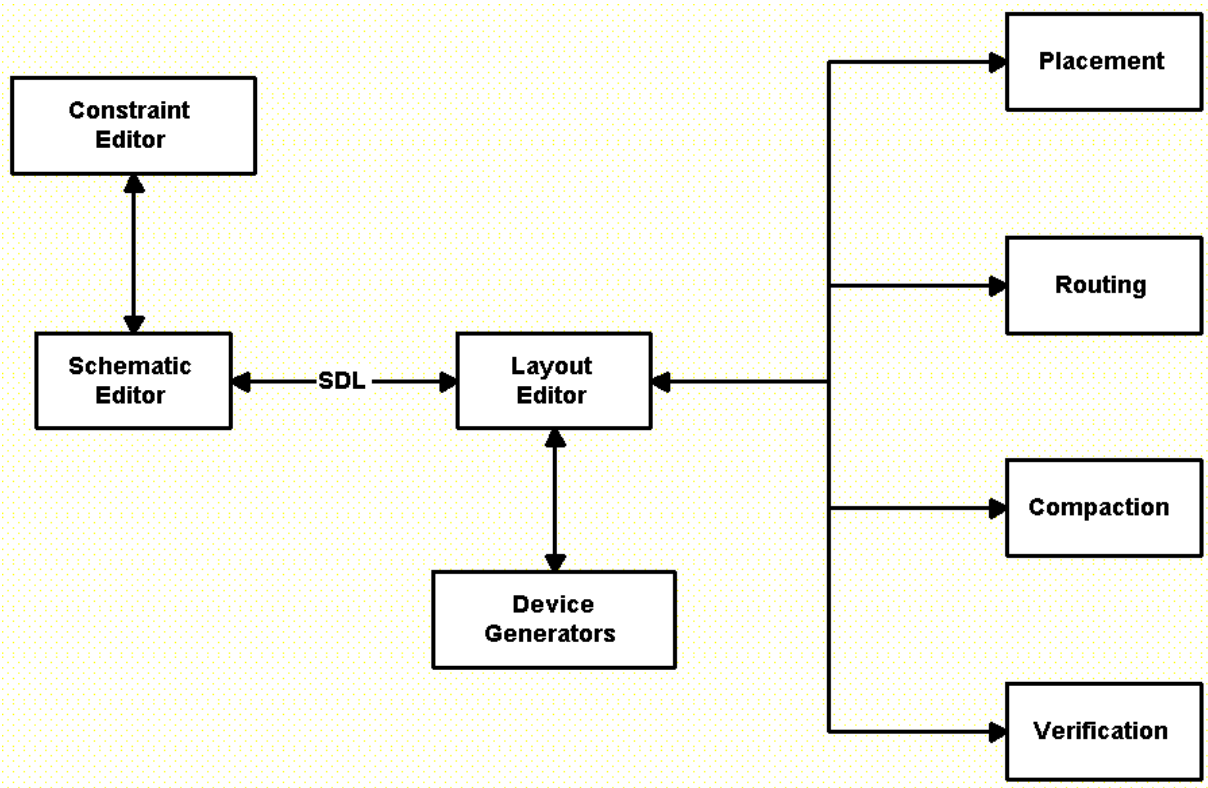

Figure 7: Overview of the schematic driven layout system

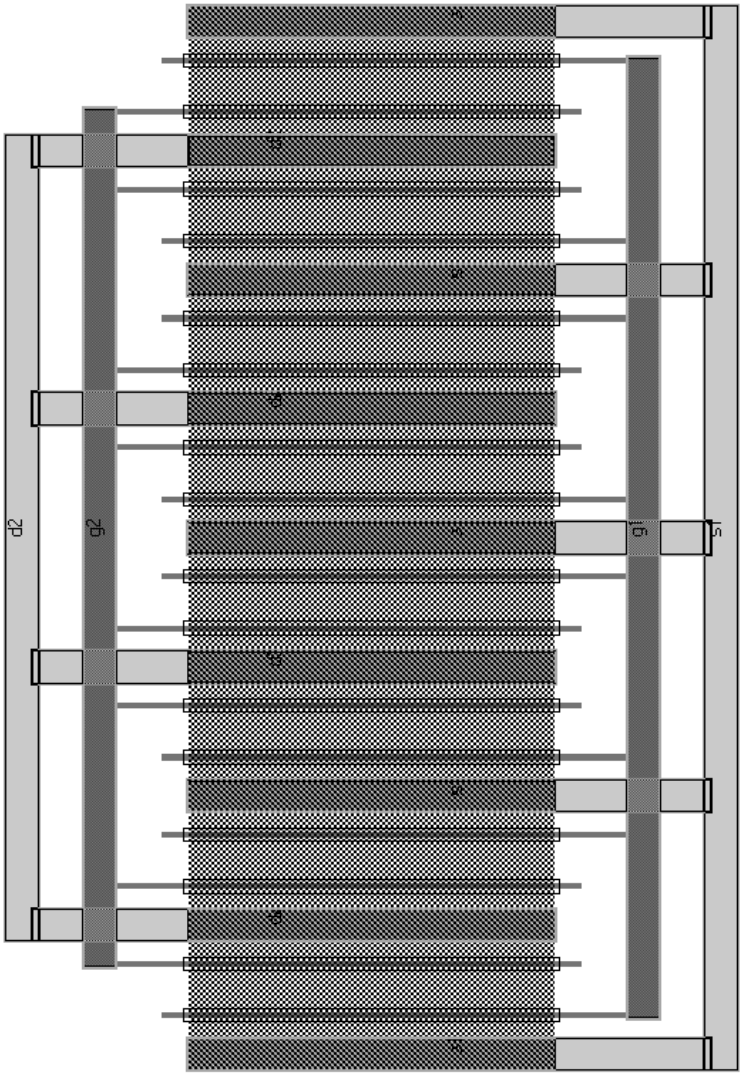

Figure 8: Cascode MOS transistor pair.

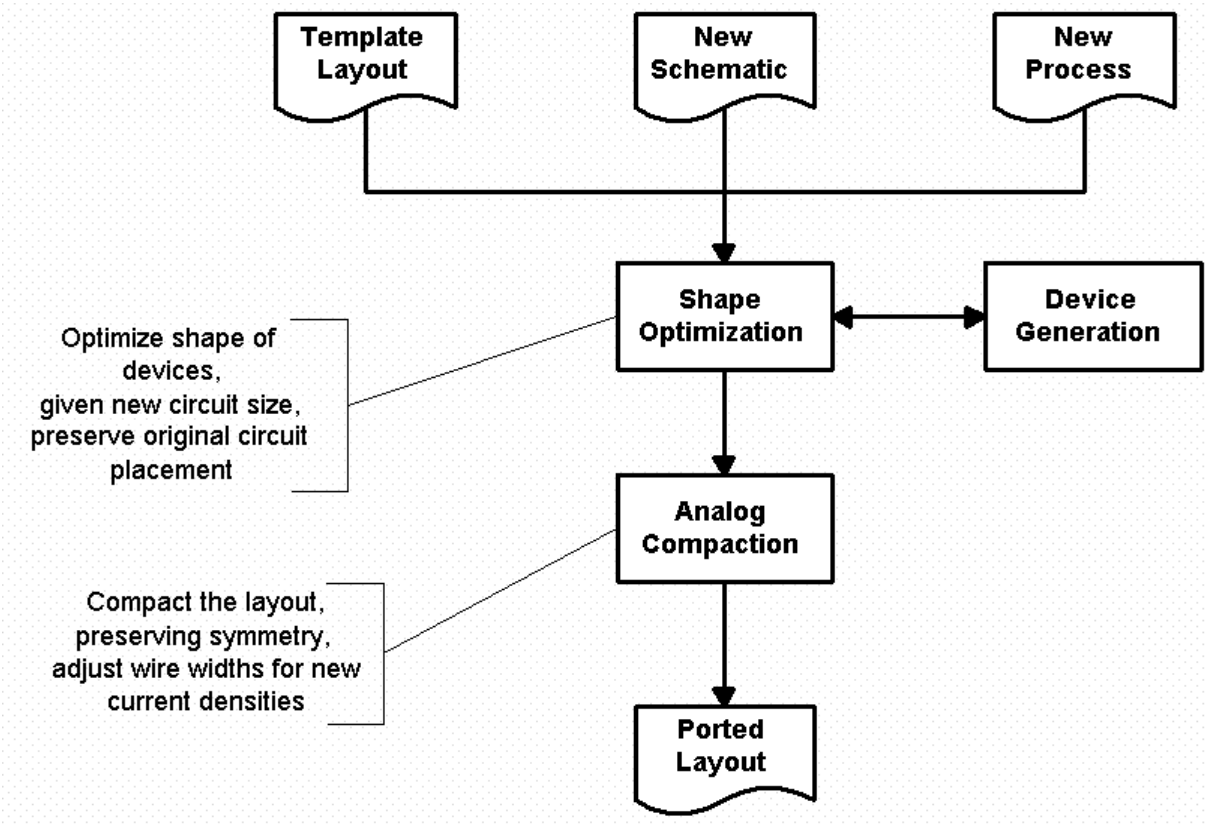

Figure 9: Overview of the template driven layout system

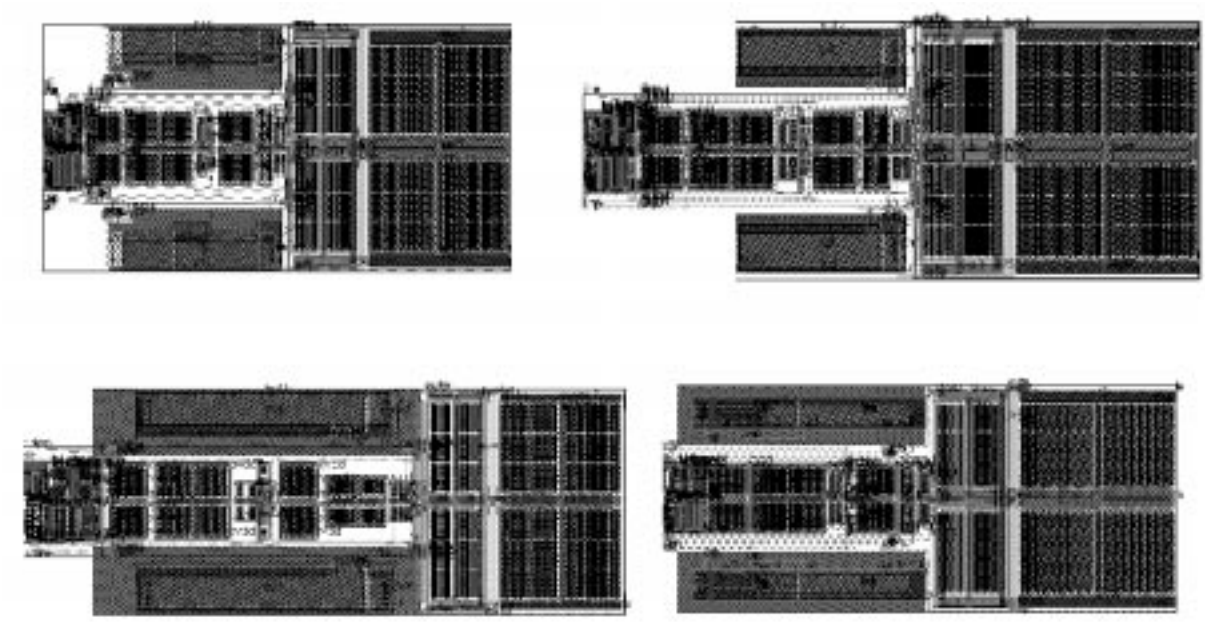

Figure 10: 4 Instances of a Differential Amplifier, automatically generated based on a layout template.

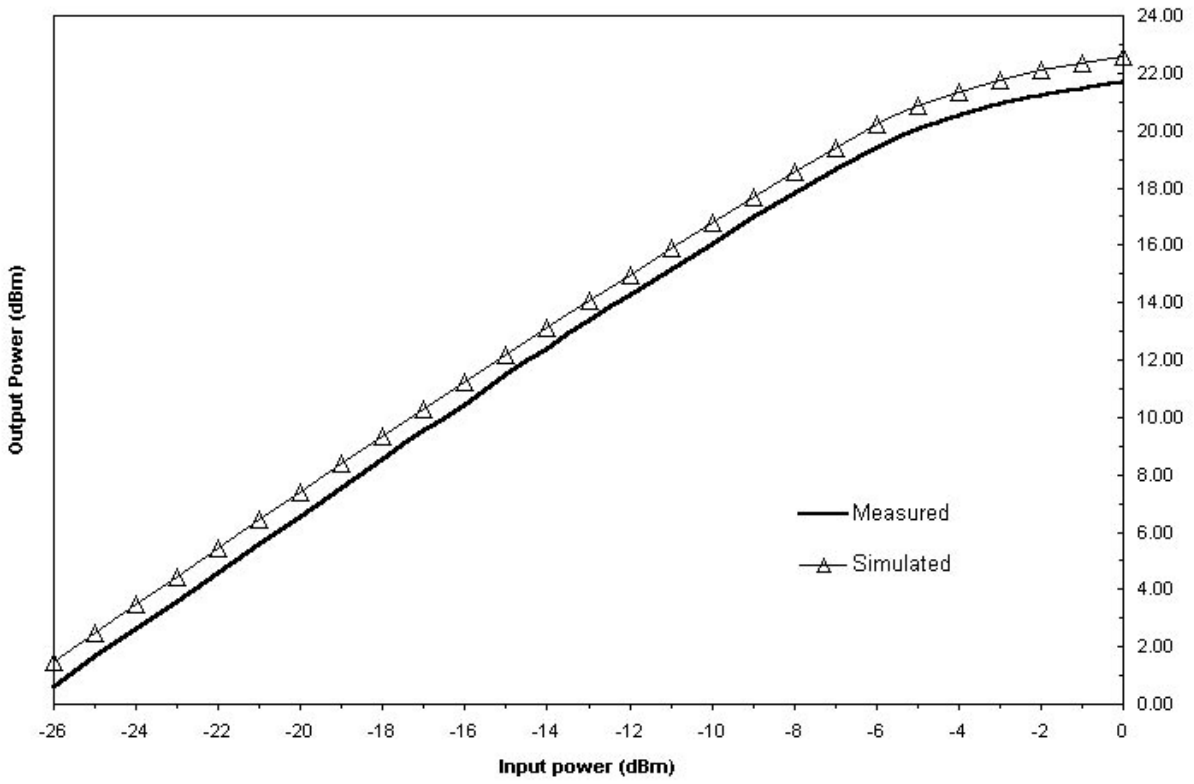

Figure 11: 2.4GHz DSS PA Gain Compression

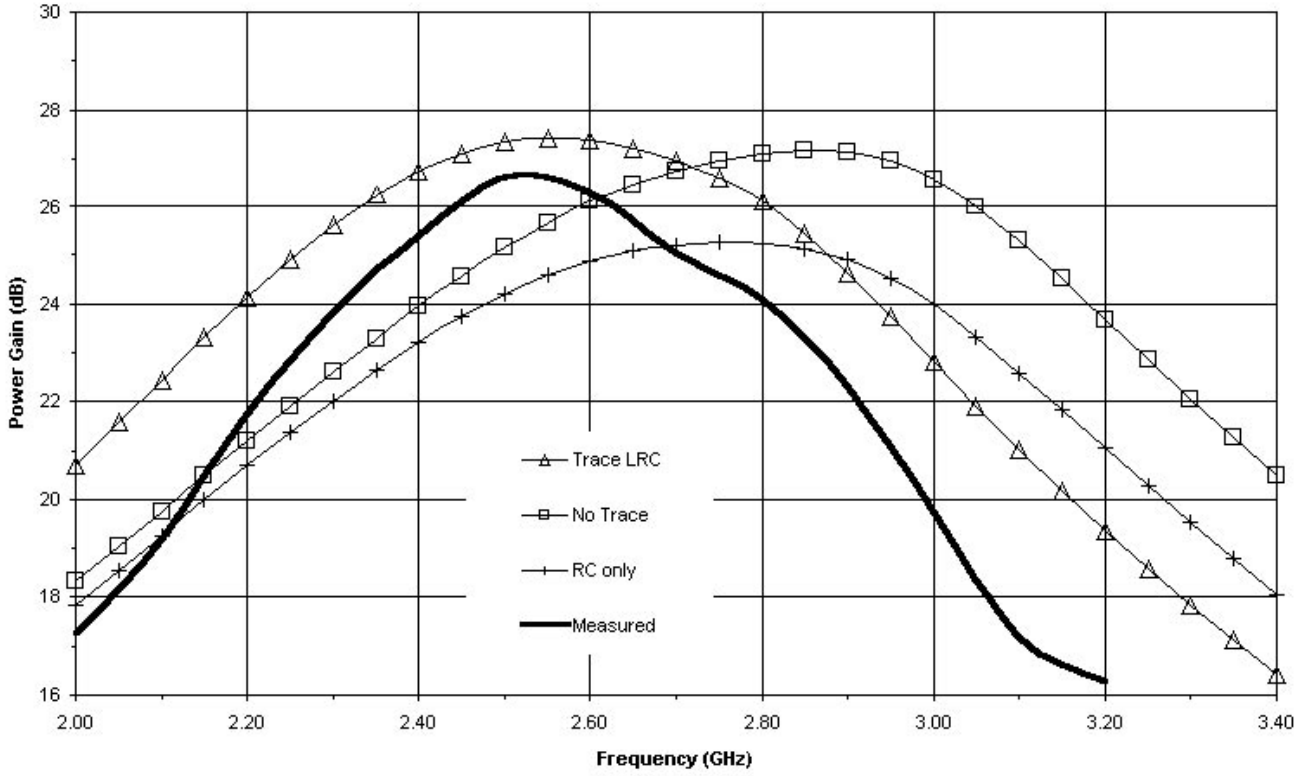

Figure 12: 2.4GHz DSS PA Frequency Responce