



Designer's Guide Consulting
Bridging the gap between design and EDA

Applying Top-Down Verification Concepts to Compact Models

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Design Challenges

- **Functionality**
 - Many standards
 - Adaptable to different end products
- **Performance**
 - Specifications and exceeding them
 - Low power
- **Cost**
 - High yield
 - Small die area
- **All before the holidays!**
 - Design productivity
 - Design quality
 - Fast ramp to volume
- **Repeatable**



Fierce Competition

ICs

Only one is designed in



Prototypes

Only one is sold



End Products



No margin for error!

Verification Issues

- Chip function
- Chip performance
- Block performance

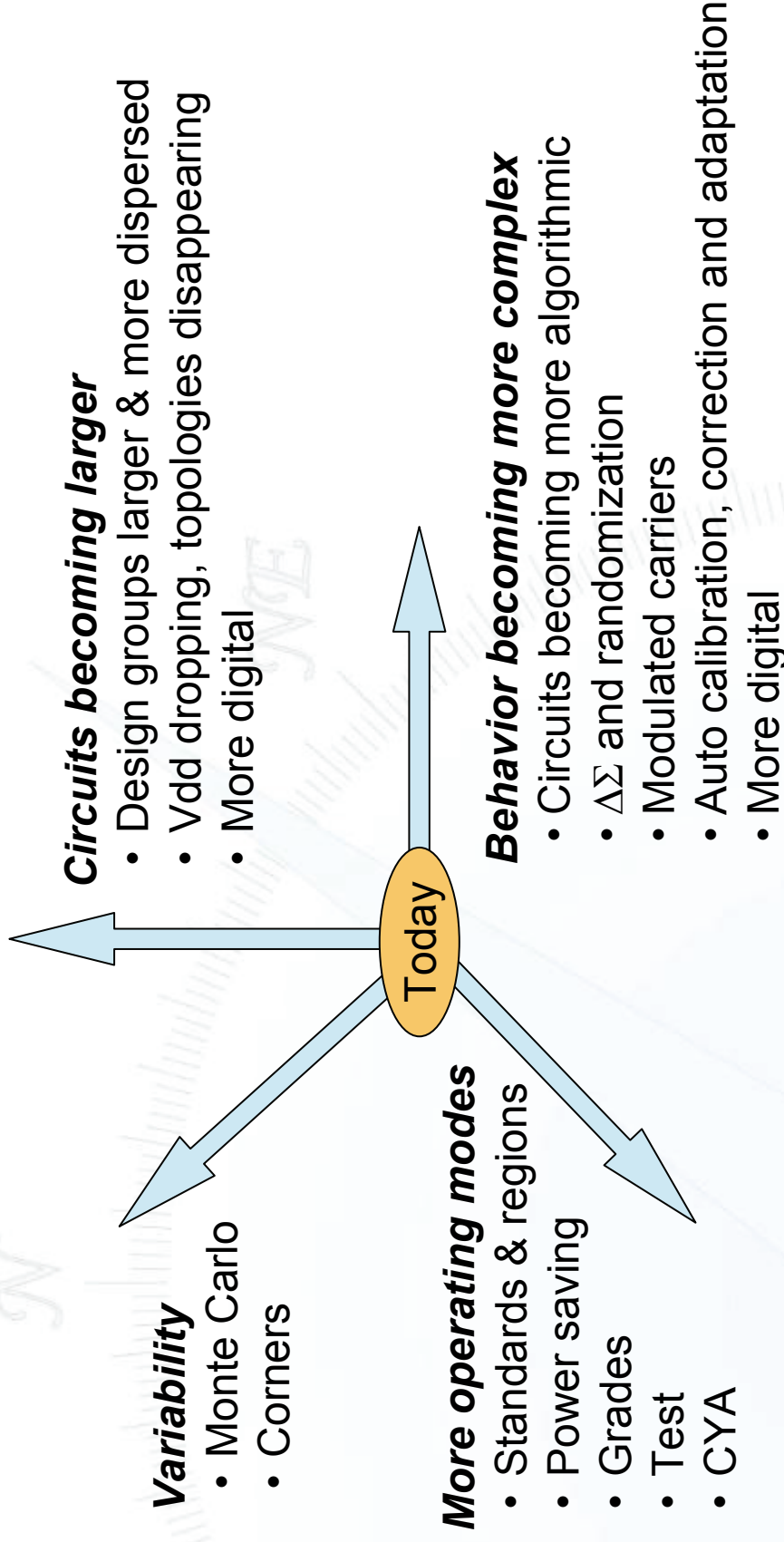


Outline

- Design Challenge
- Verification Challenge
- Addressing the Challenge
 - Methodology
 - Compact Model's Role
- Conclusion



Verification



Verification Options?

- Consider just 3 dimensions of complexity
 - Assume each is growing at Moore's law like rates (2x in 2 years)
- That is 8x every two years
 - 64x every election cycle
- Where can we find such speed-ups?
 - Improved algorithms?
 - Hardware improvements?
 - Special-purpose simulators?



Timing ~~SPICE~~ *Simulators*

- Provide 5-10x SPICE with same accuracy
 - HSim, NanoSim, UltraSim, etc.

Not with Analog!

- 0.75-2x on analog and mixed-signal
- No AC, no noise, no RF
- Sacrifice accuracy
- Not as robust



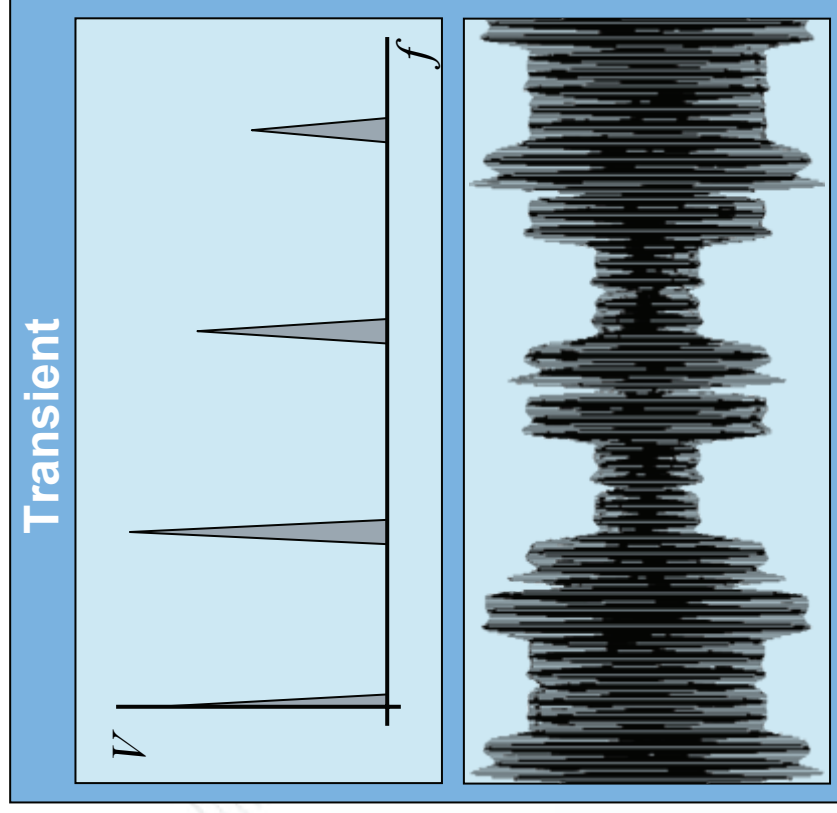
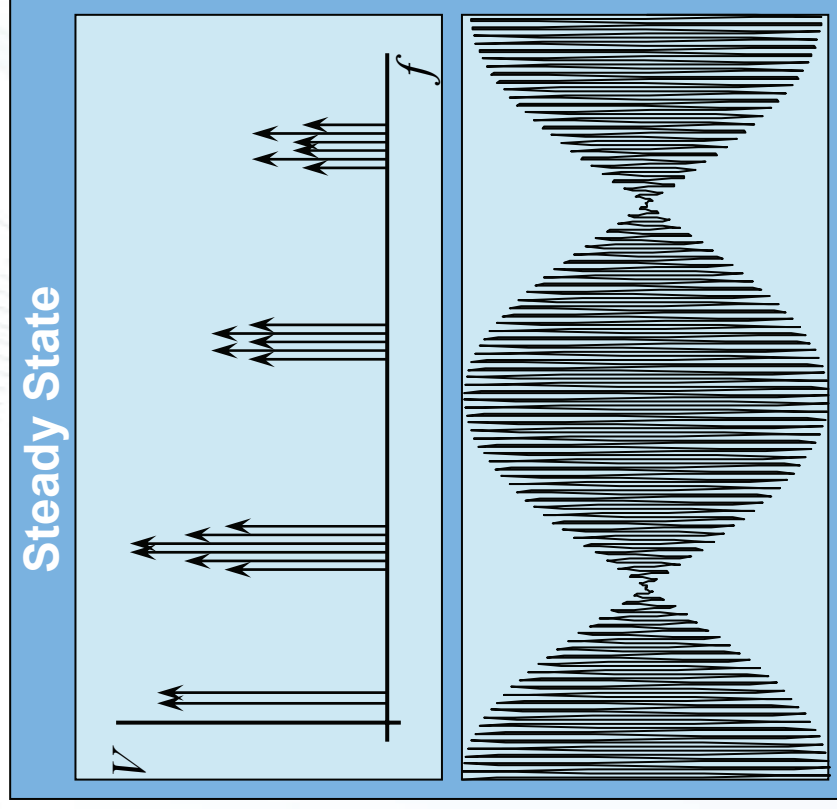
Parallel Processing

- Processor performance has leveled off
- Multi-core era begins
- However:
 - Simulation notoriously difficult to parallelize
 - Will take a while



RF Simulators

- Exploit nature of RF circuits to run efficiently
 - Assume sparse spectrum, few harmonics



Assumptions of RF Simulators

- Only one type of signal present
 - Quasiperiodic with few fundamentals (≤ 3),
 - Or slowly modulated periodic carrier
- Small number of harmonics
- Small number of oscillator modes (≤ 1)
- Near-linear signal path
- No Verilog or VHDL
 - Purely transistor level
 - Verilog-A okay if no hidden state



Consequences of Assumptions

- RF simulators provide many analyses
 - Each suitable for a small range of situations
 - SpectreRF: PSS, PAC, PXF, PNoise, PSP, Envelope, QPSS, QPAC, QPXF, QPNoise, QPSP
 - Many situations still not covered
 - Ex., semi-autonomous and poly-autonomous circuits
- *Analyses often cannot be applied to heterogeneous circuits*
 - They are too constrained!



Heterogeneous Systems

- Result from need for higher integration
 - *Leads to larger, more diverse systems*
 - Examples: Transceiver with ...
 - Synthesizer
 - Converters
- Result from more challenging requirements
 - *Leads to increasing use of error correction*
 - Examples ...
 - Adaptive filtering, biasing and predistortion
 - Offset, gain, quadrature error correction
 - Modes
 - Sub-ranging



RF Simulators

- ✓ Work well on individual functional blocks
 - Amplifiers, mixers, oscillators, filters, etc.
 - Segments of RF signal path
- ✗ Work poorly on algorithmic blocks
 - ADC, DAC, PLL (frequency synthesizer)
 - Anything $\Delta\Sigma$
- ✗ Work poorly on heterogeneous systems
 - Full transmitter or receiver
 - Digital calibration or adaptation



Verification Options?

- Improved algorithms?
 - ✘ Timing simulators
- Hardware improvements?
 - ✘ Parallel processing
- Special-purpose simulators?
 - ✘ RF simulation
- All three together ???



Transistor Only Simulation

- Full system verification occurs too late
 - Errors are expensive to fix
 - Cause redesign of blocks
 - Impacts schedule
- Does not address communication issues
 - Root cause of system level errors
- Is very expensive
 - Reduces amount of verification performed



Verification Options?

- Improved algorithms?
 - ✘ Timing simulators
- Hardware improvements?
 - ✘ Parallel processing
- Special-purpose simulators?
 - ✘ RF simulation
- All three together?
 - ✘ Transistor-level simulation
- Avoidance ???



Cost of Not Verifying

- Currently nobody fully verifies their designs
 - Is much too expensive
- Result is functional errors
 - At the interfaces
 - In the margins



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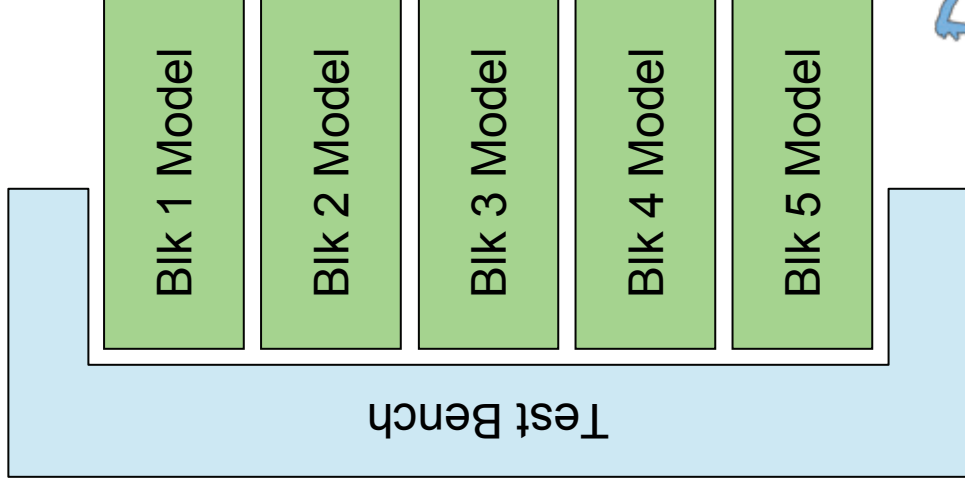
Model-Based Verification

- Replace transistor-level circuits with models
 - Run much faster
 - Available before block is designed
- Then verify that models match circuit
 - Simulate one block at a time
 - Each block can be simulated in parallel



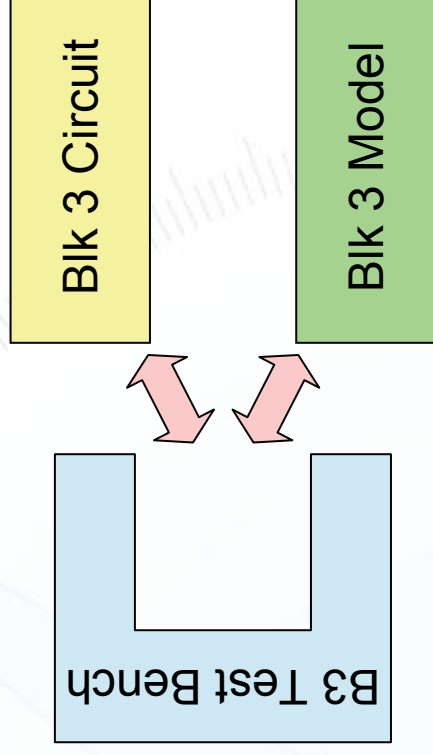
Top-Level Simulation with Models

- Verifies that performance with model meets expectations
- Verifies consistency between models



Verifying the Model

- Verifies consistency between model & circuit in detail
- If too slow, further decompose



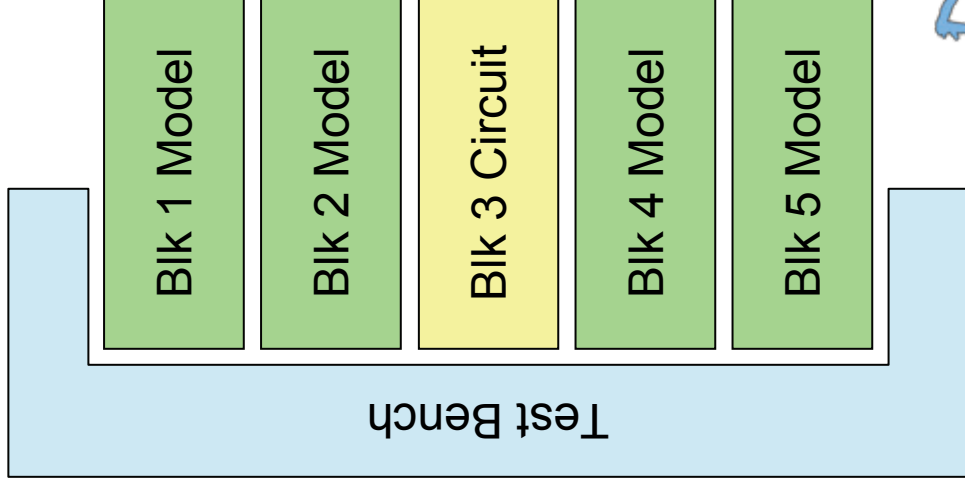
Goal for a Behavioral Model

- Model a block ...
 - Include all relevant effects with sufficient accuracy
 - Execute as fast as possible
 - Make a verification model, not a design model
 - Make a functional model, not a performance model
- Do not over model!



Mixed-Level Simulation

- Evaluate block in context of entire system
 - The system becomes the test bench for block
- Further verifies consistency between model & circuit
- Each model must be pin-accurate



This is Top-Down Verification

- Verification traceable to transistor level
- Produces both ...
 - Verified circuit
 - Verified models
 - Useful for IP delivery and reuse
- Driven by verification engineer
 - Peer to design lead



Why Top-Down Verification?

- Verifies hierarchically
 - Only approach fast enough for complex MS designs
 - Timing simulation too slow, accuracy problematic
 - RF simulation too constrained
- Improves design process
 - Reduces errors by formalizing communication
 - Moves verification earlier
- Improves test development process
 - Moves test development earlier
 - Allows test engineer to affect design



Design vs. Verification

Design

- Excel, Matlab, Models
- Topology selection
- Parameter selection
- Focus is achieving performance

*Design
Engineer*

Verification

- Functional verification
- Performance verification
- Regression testing
- Monte Carlo / corners
- Focus is on verifying functionality

*Verification
Engineer*



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Goal for a Compact Model

- Model a device ...
 - Include all relevant effects with sufficient accuracy
 - Execute as fast as possible
- Value of extra accuracy is marginal
- Value of extra speed is huge
 - It makes up 75-90% of simulation time



What is Relevant?

- It is situation specific
 - Pre-layout vs. post-layout
 - Design phase vs. verification phase
 - Application area
 - Thermal (static)
 - Thermal (dynamic)
 - Charge storage
 - Small-geometry
 - Digital
 - Proximity effects
 - High frequency
 - Noise
 - Variability
 - Latch-up
 - Leakage
 - Stress, etc.



Compact Modeling and TDV

- With top-down verification ...
 - It is important not to over model
 - Same is true of transistor models
 - Compact models still dominate simulation time
- Compact models should ...
 - Separate the concerns
 - Allow effects to be enabled on a per instance basis
 - Provide multiple levels of accuracy



Examples

- Power-up simulations
- Signal transmission simulations
- Heterogeneous systems, such as
 - RF transceiver
 - LNA, Osc, PA, synthesizer, etc.



Everything in Model

- One model that incorporates all effects
- One .model statement
- User enables/disables effects on a per instance or per block basis
 - Complex mixed-signal chips will have sections that have different concerns
- Compiler produces custom versions



Conclusion

- The design process is bifurcating into design and verification disciplines
- Design and verification engineers need different models
 - High detail and accuracy for design
 - Simple and fast for verification
- Should be the same model
 - Model compilers will produce optimized versions





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