Modeling of Jitter in Bang-Bang Clock and Data Recovery Circuits[1]

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Abstract

This paper presents an approach to analyzing bang-bang CDR loops, predicting performance aspects such as jitter transfer, jitter tolerance, jitter generation, and the bit error rate. A 1-Gb/s CDR circuit realized in 0.35-μm CMOS technology validates the theoretical results.

I. Introduction

Clock and data recovery (CDR) circuits incorporating bang-bang (binary) phase detectors (PDs) have recently found wide usage. In contrast to their linear counterparts, bang-bang PDs relax the speed and precision required of flipflops and other circuits in the signal path, reducing the complexity and the power dissipation. However, the heavily nonlinear nature of these PDs makes the loop analysis difficult.

This paper describes an approach to modeling bang-bang CDR loops with emphasis on jitter characteristics. The methodology predicts jitter transfer, tolerance, and generation as well as the bit error rate (BER). A 1-Gb/s CMOS CDR circuit is designed and fabricated as an experimental vehicle to validate the predictions.

The next section of the paper develops the basic model to be used in the analysis of the loop. Section III applies the model to jitter characteristics and BER. Section IV determines the capture range and Section V presents the experimental results.

II. Bang-bang PD Model

The ideally binary characteristic of bang-bang phase detectors in practice assumes a finite slope for a small range of input phase errors. This section quantifies this effect.

A. Metastability

When the zero-crossing points of the recovered clock fall close to those of random data, the flipflops comprising the PD may experience metastability, thereby generating an output lower than the full level for some time [Fig. 1(a)]. Depending on the linear and regenerate gains and time constants provided by the latches in the signal path, the average slope of the characteristic begins from a finite, maximum value for a phase difference, $\Delta\phi$, of zero, gradually decreasing as the average output reaches saturation [Fig. 1(b)].

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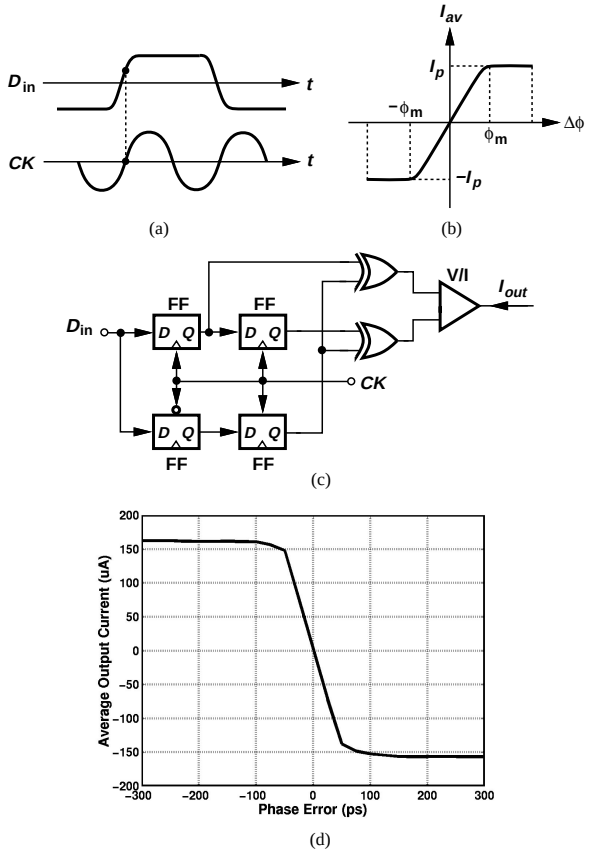


Fig. 1. Smoothing of PD characteristic due to metastability.

Figure 1(c) shows the Alexander PD [1] used in the prototype and Fig. 1(d) plots its simulated characteristic. With a regeneration time constant of 144 ps in each latch, the PD exhibits a relatively linear range for $|\Delta\phi| < \pi/10$. For any PD topology, the slope can be readily determined through transistor-level simulations while the phase difference between D_{in} and CK is varied in small steps.

B. Input and Oscillator Jitter

The binary PD characteristic is also smoothed out by the jitter inherent in the input data and the oscillator output. As illustrated in Fig. 2(a), the PD samples a level of $-V_0$ (rather than $+V_0$) when the tail of the jitter distribution shifts the clock edge to the left by more than ΔT. The average output level, $\overline{V_{PD}}$, is therefore equal to the weighted sum of positive and negative samples according to the probability of their occur-

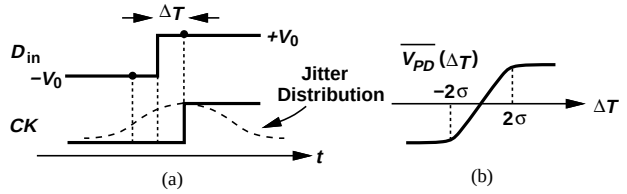


Fig. 2. Smoothing of PD characteristic due to jitter.

rence:

$$\overline{V_{PD}}(\Delta T) = V_0 \int_{+\Delta T}^{+\infty} p(x)dx - V_0 \int_{-\infty}^{+\Delta T} p(x)dx, \qquad (1)$$

where $p(x)$ denotes the probability density function of jitter. Since the total area under p(x) is equal to unity, we have

$$\overline{V_{PD}}(\Delta T) = V_0 - 2V_0 \int_{-\infty}^{+\Delta T} p(x)dx. \qquad (2)$$

For example, if $p(x)$ is Gaussian with a standard deviation (rms jitter) of σ, then $\overline{V_{PD}}(\Delta T)$ exhibits a relatively linear range for $|\Delta T| < 2\sigma$ [Fig. 2(b)]. For a PD characteristic smoothed out by metastability, it can be proved that the overall result including the effect of jitter is expressed as:

$$\overline{V_{PD,tot}}(\Delta T) = \int_{-\infty}^{+\infty} \overline{V_{PD}}(x)p(x - \Delta T)dx. \qquad (3)$$

If the rms jitter is relatively small, only the "corners" of the characteristic are smoothed by the jitter.

Figure 3 depicts the resulting CDR model. The high gain of bang-bang PDs obviates the need for charge pumps, allowing the use of a low-speed voltage-to-current (V/I) converter. Thus, the characteristic shown in Fig. 3(b) displays the average output current of the V/I converter as a function of $\Delta\phi$. Note that I_{av} and I_p can include the effect of data transition density as a simple scaling factor.

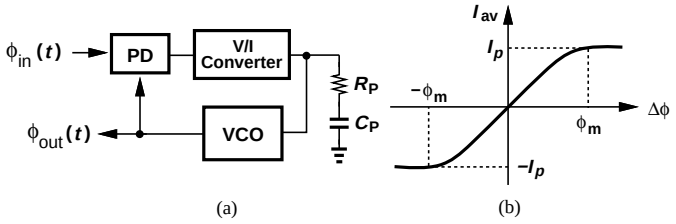


Fig. 3. CDR loop model.

III. Jitter Analysis

A. Jitter Transfer

Jitter transfer represents the response of a CDR loop to jitter, $\phi_{in}(t) = \phi_{in,p}\cos\omega_\phi t$. If $\phi_{in,p} < \phi_m$, then the PD operates in the linear region, yielding a standard second-order system. As $\phi_{in,p}$ exceeds ϕ_m, the phase difference between the input and output may also rise above ϕ_m, leading to nonlinearity. At low jitter frequencies, $\phi_{out}(t)$ still tracks $\phi_{in}(t)$ closely, $|\Delta\phi| < |\phi_m|$, and $|\phi_{out}/\phi_{in}| \approx 1$. As ω_ϕ increases, so does $\Delta\phi$, demanding that the V/I converter pump a larger current into the loop filter. However, since the available current beyond the linear PD region is constant, large and fast variation of ϕ_{in} results in "slewing".

To study this phenomenon, let us assume $\phi_{in,p} \gg \phi_m$ as an extreme case so that $\Delta\phi$ changes polarity in every half cycle of ω_ϕ, requiring that $I_{V/I}$ alternately jump between $+I_p$ and $-I_p$ (Fig. 4). Since the loop filter capacitor is typically large, this current waveform introduces a binary modulation of the

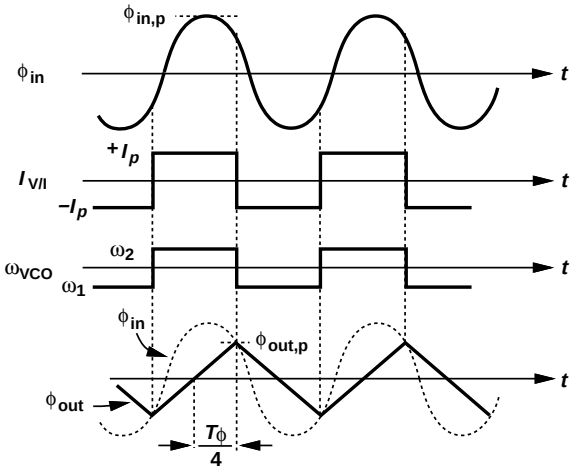


Fig. 4. Slewing in a CDR loop.

VCO frequency and hence a triangular variation of the output phase. The peak value of ϕ_{out} results after integration of the control voltage for a duration of $T_\phi/4$, where $T_\phi = 2\pi/\omega_\phi$; that is, $\phi_{out,p} = (K_{VCO}I_pR_p)(T_\phi/4)$ and

$$|\frac{\phi_{out,p}}{\phi_{in,p}}| = \frac{\pi K_{VCO}I_pR_p}{2\phi_{in,p}\omega_\phi}. \qquad (4)$$

This equation both expresses the dependence of the jitter transfer upon the input jitter amplitude and reveals that ϕ_{out}/ϕ_{in} falls at a rate of 20 dB/dec as a function of ω_ϕ.

The -3-dB bandwidth of the jitter transfer occurs in the vicinity of the frequency at which slewing begins,i.e., the output jitter amplitude falls below that at the input. The value of ω_ϕ that gives $\phi_{out,p} = \phi_{in,p}$ is equal to:

$$\omega_{-3dB} = \frac{\pi K_{VCO}I_pR_p}{2\phi_{in,p}}. \qquad (5)$$

We thus approximate the overall jitter transfer function as

$$\frac{\phi_{out,p}}{\phi_{in,p}}(s) = \frac{1}{1 + \dfrac{s}{\omega_{-3dB}}}, \qquad (6)$$

observing that the jitter bandwidth is inversely proportional to the input jitter amplitude and independent of C_p so long as this capacitor is sufficiently large.

Figure 5 plots the behavior of the jitter transfer for different input jitter amplitudes. The transfer approaches that of a linear loop as $\phi_{in,p}$ decreases toward ϕ_m.

It is interesting to note that the jitter transfer of slew-limited CDR loops exhibits negligible peaking. This is because slew-

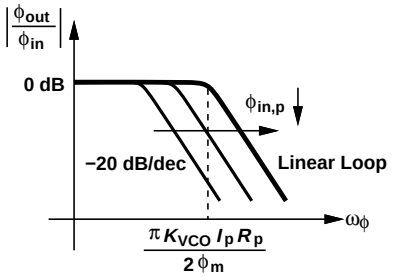


Fig. 5. Jitter transfer function of a bang-bang CDR.

ing and hence variation of the output jitter amplitude are monotonic functions of the jitter frequency. This is verified by simulations.

B. Jitter Tolerance

Jitter tolerance is defined as the maximum input jitter that a CDR loop can tolerate without increasing the bit error rate at a given jitter frequency. As the phase error, $\phi_{in} - \phi_{out}$, approaches π [half unit interval (UI)], BER begins to rise.

It is important to recognize that a bang-bang loop *must* slew if it incurs errors. With no slewing, the phase difference between the input and output falls below $\phi_m (\ll \pi)$, and the data is sampled correctly. Figure 6(a) shows an example where ϕ_{out} slews and $\phi_{in,p}$ is chosen such that $\Delta\phi_{max} = \pi$. Thus, a relationship is sought that expresses $\phi_{in,p}$ in terms of ω_ϕ while the maximum phase error is equal to 0.5 UI.

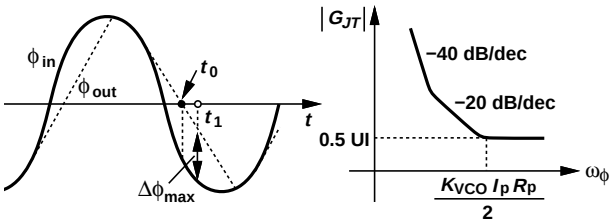


Fig. 6. (a) Slewing in jitter tolerance test, (b) jitter tolerance of a bang-bang CDR.

Figure 6(a) reveals that $\Delta\phi_{max}$ occurs at t_1, but the jitter tolerance calculation can be greatly simplified by assuming $\Delta\phi(t_0) \approx \Delta\phi(t_1)$. If ϕ_{out} slews for the most part of the period, we have

$$\Delta\phi_{max} \approx \frac{\sqrt{4\omega_\phi^2\phi_{in,p}^2 - \pi^2 K_{VCO}^2 I_p^2 R_p^2}}{2\omega_\phi}. \quad (7)$$

Equating $\Delta\phi_{max}$ to π yields

$$|G_{JT}| = \frac{\pi\sqrt{4\omega_\phi^2 + K_{VCO}^2 I_p^2 R_p^2}}{2\omega_\phi}. \quad (8)$$

As expected, $|G_{JT}|$ falls at a rate of 20 dB/dec for $\omega_\phi < K_{VCO} I_p R_p/2$ and approaches 0.5 UI afterwards.

The above analysis has followed the same assumptions as those in Fig. 4, namely, the change in the control voltage is due to $I_{V/I} R_p$ and the voltage across C_p remains constant. At jitter frequencies below $(R_p C_p)^{-1}$, however, this condition is violated, leading to "nonlinear slewing" at the output. In this regime, or if C_p is reduced, $|G_{JT}|$ falls at a rate of approximately 40 dB/dec [Fig. 6(b)].

C. Jitter Generation

The sources that generate jitter in a CDR loop include phase noise of the VCO, noise of the PD, ripple on the control line, and supply and substrate noise. The PD used in this study is based on the Alexander topology [1], providing binary characteristics but, ideally, injecting no current into the loop filter during long runs. Thus, the effect of the ripple is negligible. We consider the VCO phase noise here.

For low-frequency or small VCO jitter, the PD operates linearly, yielding a second-order high-pass transfer function for the VCO phase noise that can be simplified if the damping factor is large:

$$\frac{\phi_{out}}{\phi_{in}}(s) \approx \frac{s}{s + 2\zeta\omega_n}, \quad (9)$$

where $\omega_n = \sqrt{I_p K_{VCO}/C_p}$ and $\zeta = R_p\sqrt{I_p C_p K_{VCO}}/2$. At moderate jitter frequencies, as the VCO jitter amplitude approaches ϕ_m, the V/I output current reaches saturation, allowing a greater phase error at the output. Thus, ϕ_{out}/ϕ_{VCO} begins to rise at a greater rate ($\propto \omega_\phi^{1.5\sim2}$). Illustrated in Fig. 7(b), this phenomenon amplifies large VCO jitter excursions and must be avoided by proper design.

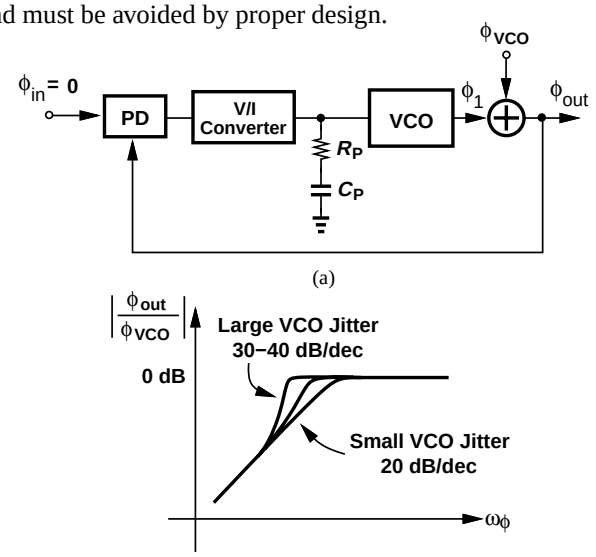


Fig. 7. Effect of VCO phase noise.

D. Bit Error Rate

To compute the BER, we employ the model depicted in Fig. 8, where the jitter of the VCO and the PD is represented as additive phase terms with a Gaussian distribution. The standard deviations σ_{VCO} and σ_{PD} are obtained by integrating their respective spectra, e.g., in SpectreRF, and are subsequently lumped into a recovered clock jitter: $\sigma_{tot} = \sqrt{\sigma_{VCO}^2 + \sigma_{PD}^2}$. If the jittery clock edge deviates from the middle of the input

data eye by more than half a bit period, an error occurs:

$$BER = 2\int_{T_b/2}^{\infty} \frac{1}{\sqrt{2\pi\sigma_{tot}^2}} e^{-\frac{x^2}{2\sigma_{tot}^2}}\, dx \quad (10)$$

$$= 2Q(\frac{T_b}{2\sigma_{tot}}). \quad (11)$$

Note that this method is by far more computationally efficient than direct simulation of BER.

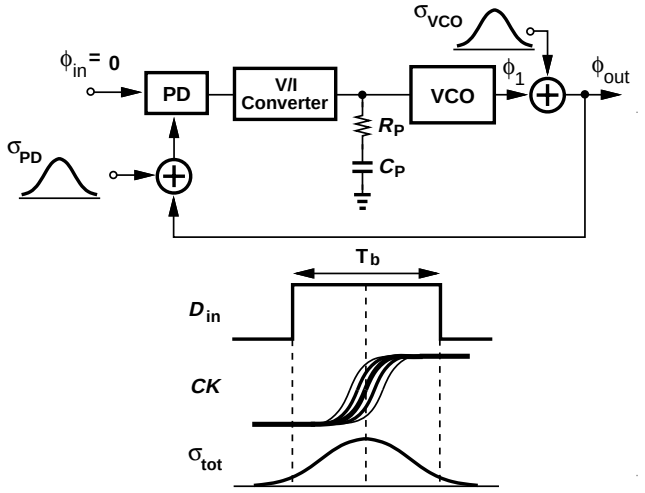
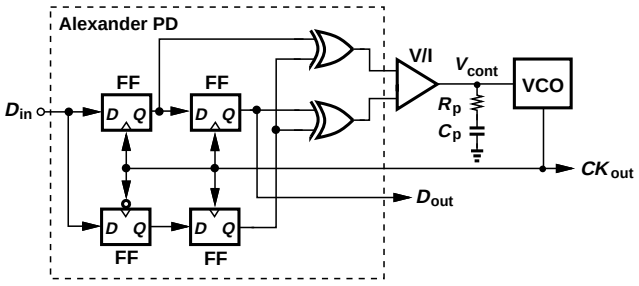


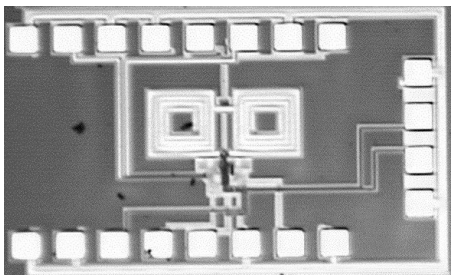
Fig. 8. Calculation of BER.

IV. Experimental Results

A CDR circuit has been designed and fabricated in a 0.35-μm CMOS technology to validate the above analysis and modeling techniques. Figure 9(a) shows the CDR architecture and Fig. 9(b) the die photograph. The LC VCO employs cross-coupled transistors and MOS varactors.



(a)



(b)

Fig. 9. (a) CDR architecture, (b) die photo.

Figure 10 shows the theoretical and measured jitter transfer functions for input jitter amplitudes of 0.25, 0.5, and 1 UI. A reasonable agreement is obtained. The jitter peaking in experimental results is less than 0.25 dB. Figure 11 plots the simulated and measured jitter tolerance. The high-frequency deviation results from internal device and input data noise.

Figure 12 depicts the recovered clock jitter, suggesting an rms value of 4.77 ps and peak-to-peak value of 33 ps. The rms value predicted by the model is 4.21 ps. Owing to the very low jitter (0.033 UI_{pp}), the BER of the prototype cannot be measured.

References

[1] J. D. H. Alexander, "Clock Recovery from Random Binary Data," *Electronics Letters*, vol. 11, pp. 541-542, Oct. 1975.

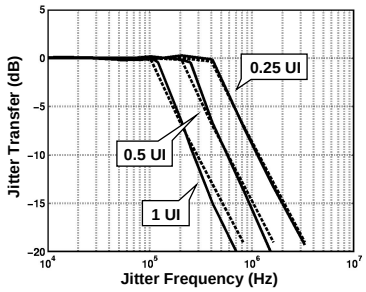


Fig. 10. Jitter transfer from theory (dashed) and measurements (solid).

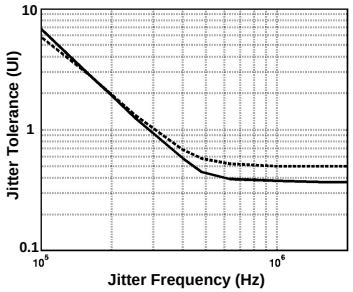


Fig. 11. Jitter tolerance from simulation (dashed) and measurement (solid).

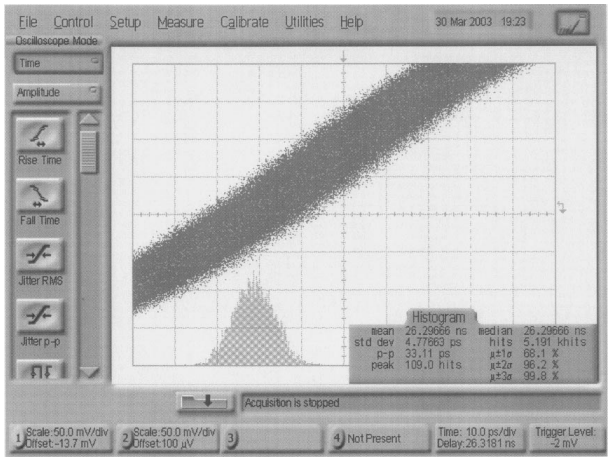


Fig. 12. Recovered clock histogram.